EK-1184A-MG-001

PDP-11/84 System Maintenance Guide

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PDP-11/84 System Maintenance Guide

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CHAPTER 1
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1.1 INTRODUCTION

The major cabinet and box components are shown in Figures 1-1 and 1-2. Table 1-1 briefly describes the basic A-series system components. Table 1-2 specifies the module revisions and options used with P-series systems.

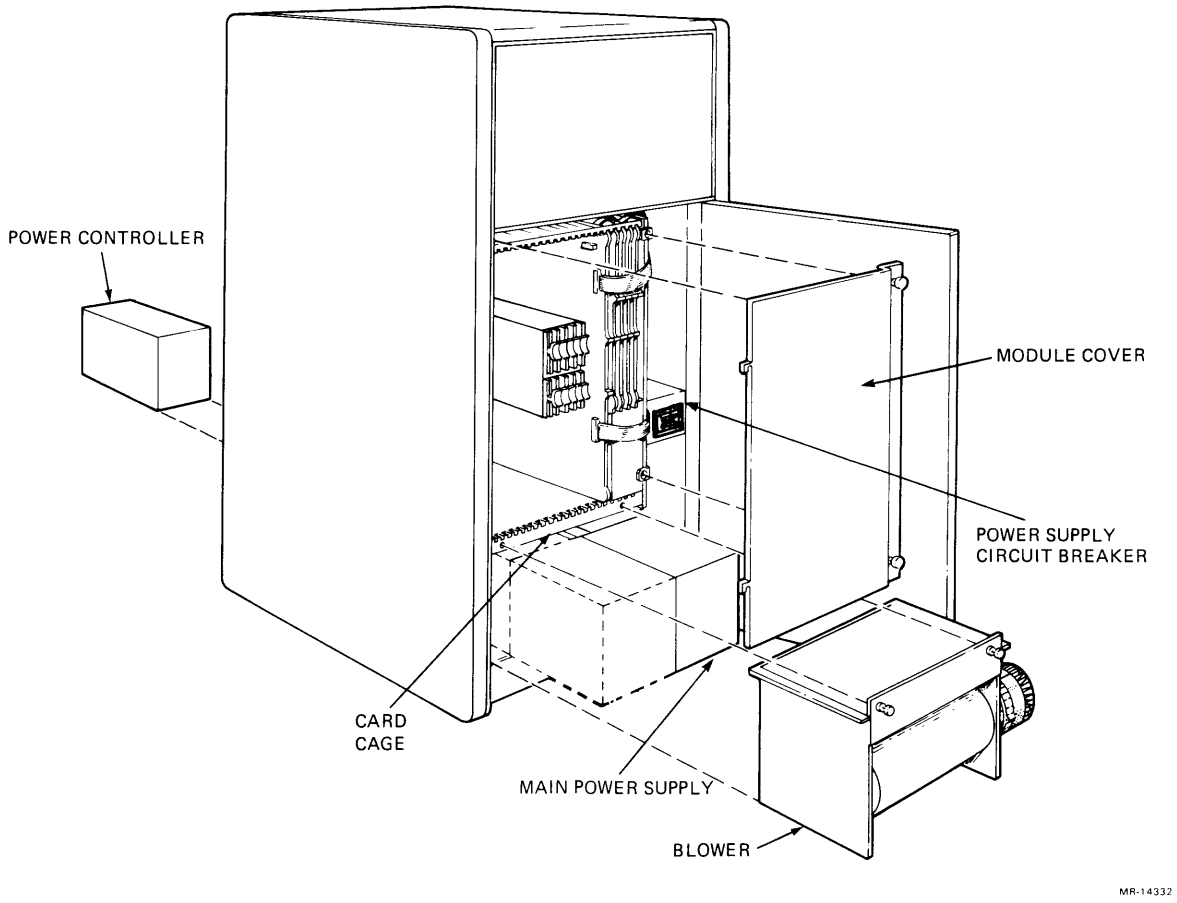

Figure 1-1 Basic Cabinet Hardware Components

IMPORTANT

After replacing a KDJ11-BF CPU module, reset the Set-up feature selections of the replacement module as recorded on the Set-up Parameter Worksheets. The worksheets should be stored with the system documentation.

If the worksheets are not available, fill in the worksheets (contained in Appendix B) as specified by the customer. Remove the worksheets from the appendix and store them with the system documentation.

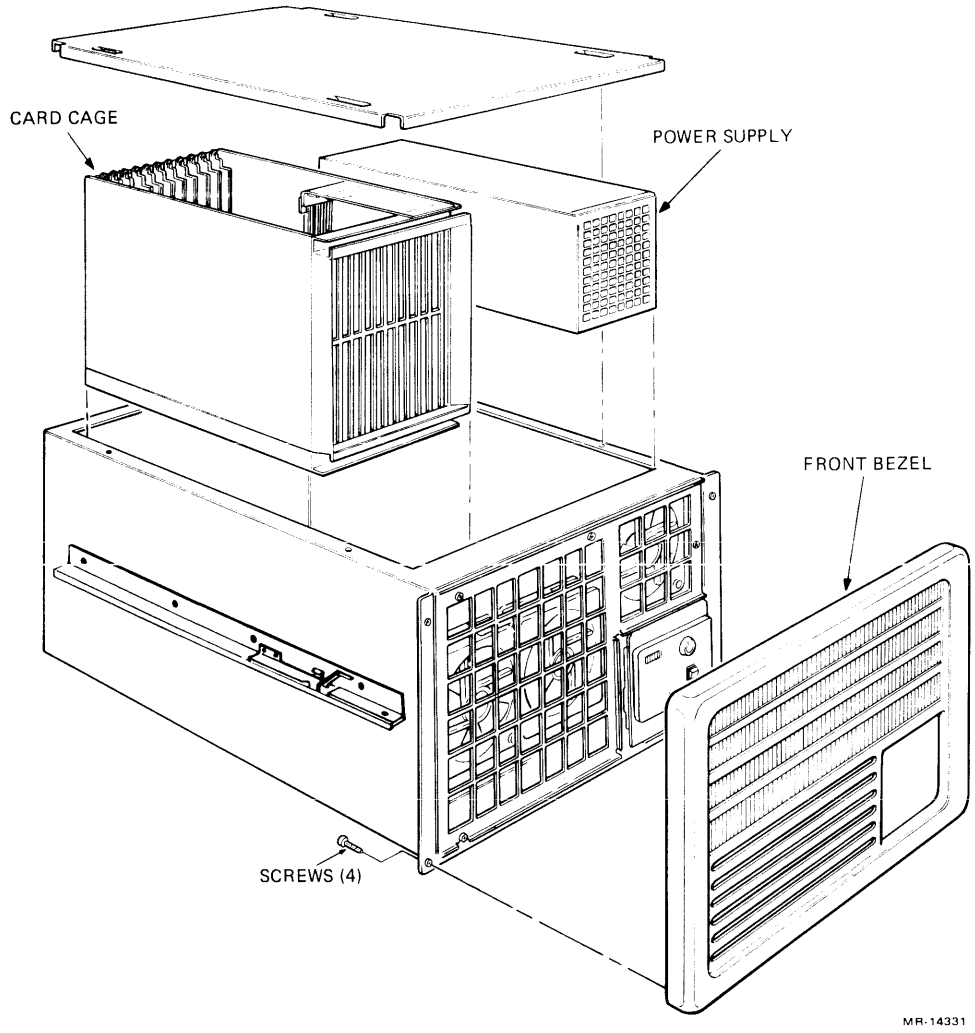

Figure 1-2 Basic Box Hardware Components

Table 1-1 Basic A-Series Components

Component (Part Number)	Description
KDJ11-BF (M8190-AE)	CPU – FPA module
KTJ11-B (M8191)	UBA module
MSV11-JB (M8637-BA)	1 Mbyte ECC memory module
MSV11-JC (M8637-CA)	2 Mbyte ECC memory module
Terminator (M9302)	UNIBUS terminator module
MDM (M7677-YA) *	Monitor and distribution module
Load module (M7556)	Minimum load module
877-D	Cabinet power controller 120 Vac
877-F	Cabinet power controller 240 Vac
H7202-KA	Main backplane power supply
H7202-KB	Expansion backplane power supply
54-16508-01	Console serial line board
70-20650-01	CPU backplane assembly
70-21888-01	Front panel assembly
12-22001-01	Cabinet blower
12-22271-02	Box fan
Options	
H7231-E	Cabinet battery-backup unit
H7231-F	Box battery-backup unit
DD11-CK	4-slot backplane
DD11-DK	9-slot backplane

* M7677-YA must be installed if the system contains the H7231-E BBU option.

The following list specifies the P-series module revisions, and the supported and unsupported options.

- KDJ11-BC (M8190), CPU module (no FPA)
- MSV11-RA (M7458-A), 1 Mbyte parity memory module
- M7677 MDM module
- DD11-CK 4-slot backplane (supported option)
- DD11-DK 9-slot backplane (supported option)

1.2 SYSTEM SPECIFICATIONS

The following tables list the PDP-11/84 system specifications. Table 1-2 through Table 1-4 list the cabinet specifications; Table 1-5 through Table 1-7 list the box specifications.

Table 1-2 Cabinet Environmental Specifications

Characteristic	Description
Temperature	
Operating	10°C - 40°C (50°F - 104°F)
Nonoperating (storage)	−40°C - 66°C (−40°F - 151°F)
Humidity	
Operating	10% to 90% with maximum wet bulb temperature 28°C (82°F) and a minimum dew point 2°C (36°F) noncondensing.
Vibration	
Operating	5 Hz to 22 Hz: 0.01 in DA; 22 Hz to 500 Hz 0.25 Gpk. Sweep rate of 1.0 octave/min. All three axes.
Nonoperating (packed for shipment)	Vertical axis random vibration: 1.4 Grms overall from 10 Hz to 200 Hz; duration: 1 hr each axis.
Altitude	
Operating	0 to 2.4 km (8000 ft)
Nonoperating	9.1 km (30,000 ft)
Maximum operating with altitude	Maximum operating (40°C) should be reduced 1.8°C/1000 m (1°F/1000 ft) above sea level.
Shock	
Operating	10 Gpk for 10 ms (+3 ms), ½ sine wave, vertical axis only.
Nonoperating (packaged for shipment)	Flat drop from a 15.2 cm (6 inch) height, three drops total (vertical direction only).

Table 1-3 Cabinet Mechanical Specifications

Characteristic	Description
Height	105.7 cm (41.64 inches)
Width	53.9 cm (21.25 inches)
Length	76.2 cm (30 inches)
Weight (packed)	182.2 kg (401 lb)
Weight (unpacked)	150.5 kg (331 lb)

Table 1-4 Cabinet Electrical Specifications

Characteristics	Description
120 Vac operation	
Line voltage	93 Vrms – 132 Vrms, single-phase, 2-wire and ground (120 Vrms nominal)
Frequency	47.5 Hz – 63 Hz
Current (ac)	13.5 Arms maximum at 120 Vac
Power factor	Greater than 0.60 at full output load and low input voltage (93)
Startup current	100 A, 0.16 μs duration
Inrush current	160 A (peak) maximum at 120 Vac, 0.16 μs duration
Power	2880 V-A maximum*
Btu	2218
240 Vac operation	
Line voltage	186 Vrms – 264 Vrms, single-phase, 2-wire and ground (240 Vrms nominal)
Frequency	47.5 Hz – 63 Hz
Current (ac)	6.7 Arms maximum at 240 Vac
Power factor	Greater than 0.60 at full output load and low input voltage (186 Vac)
Startup current	50 A, 0.16 μs duration
Inrush current	160 A (peak) maximum at 240 Vac, 0.16 μs duration
Power	2880 V-A maximum*
Btu	2218
Noise transient (both line voltages)	
High-energy transients	1 kV peak spike containing not more than 0.2 W of energy per spike
Conducted noise	CW-10 kHz to 30 MHz, 3 Vrms

* Including mass storage devices

Table 1-5 Box Environmental Specifications

Characteristic	Description
Temperature	
Operating	5°C - 50°C (41°F - 122°F)
Nonoperating (storage)	−40°C - 66°C (−40°F - 151°F)
Humidity	
Operating	10% to 95% with maximum wet bulb temperature. 32°C (82°F) and a minimum dew point 2°C (36°F) noncondensing.
Vibration	
Operating	5 Hz to 30 Hz: 0.01 in DA; 30 Hz to 500 Hz: 0.5 Gpk. Sweep rate of 1.0 octave/min. All three axes.
Nonoperating (packed for shipment)	Vertical axis random vibration: 0.687 Grms overall from 10 Hz to 200 Hz; duration: 1 hr each.
Altitude	
Operating	0 to 2.4 km (8000 ft)
Nonoperating	9.1 km (30,000 ft)
Shock	
Operating	10 Gpk for 10 ms (+3 ms), ½ sine wave, vertical axis only.
Nonoperating	Flat drop from a 15.2 cm (6 inch) height, three drops total (vertical direction only).
Maximum operating with altitude	Maximum operating 40°C (104°F) should be reduced 1.8°C/1000m (1°F/1000 ft) above sea level.

Table 1-6 Box Mechanical Specifications

Characteristic	Description
Height	26 cm (10.44 inches)
Width	47 cm (19 inches)
Length	67.5 cm (27 inches)
Weight (packed)	59 kg (130 lb)
Weight (unpacked)	42.75 kg (95 lb)

Table 1-7 Box Electrical Specifications

Characteristic	Description
120 Vac operation	
Line voltage	90 Vrms – 132 Vrms, single-phase, 2-wire and ground (120 Vrms nominal).
Frequency	47.5 Hz – 63 Hz
Current (ac)	8.0 Arms maximum at 120 Vac
Power factor	Greater than 0.60 at full output load and 120 Vac nominal input voltage.
Startup current	50 A, 0.16 μs duration
Inrush current	80 A (peak) maximum at 120 Vac, 0.16 μs duration.
Power	650 W maximum
Btu	2218
240 Vac operation	
Line voltage	180 Vrms – 264 Vrms, single-phase, 2-wire and ground (240 Vrms nominal).
Frequency	47.5 Hz – 63 Hz
Current (ac)	5.0 A (rms) maximum at 240 Vac
Power factor	Greater than 0.60 at full output load and 240 Vac nominal input voltage.
Startup current	50 A, 0.16 μs duration
Inrush current	80 A (peak) maximum at 240 Vac, 0.16 μs duration.
Power	650 W maximum
Btu	2218
Noise transient (both line voltages)	
High-energy transients	1 kV peak spike containing not more than 0.2 W of energy per spike.
Conducted noise	CW-10 kHz to 30 MHz, 3 Vrms

1.3 PRODUCT VARIATIONS

Table 1-8 describes the A-series system variations.

Table 1-8 A-Series Product Variations

Variation	Description
11/84-AA	KDJ11-BF, MSV11-JB 1 Mbyte 26.7 cm (10.5 inch) box, 120 Vac
11/84-AB	KDJ11-BF, MSV11-JB 1 Mbyte 26.7 cm (10.5 inch) box, 240 Vac
11/84-BA	Same as -AA except MSV11-JC 2 Mbyte
11/84-BB	Same as -AB except MSV11-JC 2 Mbyte
11X84-AA	KDJ11-BF, MVS11-JB 1 Mbyte 105.7 cm (40 inch) cabinet, 120 Vac
11X84-AB	KDJ11-BF, MSV11-JB 1 Mbyte 105.7 cm (40 inch) cabinet, 240 Vac
11X84-BA	Same as -AA except MSV11-JC 2 Mbyte
11X84-BB	Same as -AB except MSV11-JC 2 Mbyte

1.4 RELATED DOCUMENTS

Table 1-9 PDP-11/84 Related Documents

Document Title		Order Number
PDP-11 Bus Handbook		EB-17525-20
PDP-11/84-P Technical Manual		EK-PDP84-TM
PDP-11/84-A Technical Manual		EK-1184A-TM
PDP-11/84 Site Preparation, Unpacking and Installation Guide		EK-PDP84-IN
PDP-11/84-P System Field Maintenance Print Set	Cabinet: Box:	MP-02011 MP-02015
PDP-11/84-A System Field Maintenance Print Set	Cabinet: Box:	MP-02199 MP-02198
KDJ11-B User Guide		EK-PDP84-UG
MSV11-J User Guide		EK-MSV1J-UG
MSV11-R User Guide		EK-MSV1R-UG
Chipkit Handbook		EJ-01387-92
DCJ11 User Guide		EK-DCJ11-UG
Microsystem Handbook		EB-2605-41/85

Printed copies of the above listed documents may be ordered from:

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Northboro, Massachusetts 01532
ATTN: Printing and Circulation Services (NR2/M15)
Customer Services Section

CHAPTER 2
DIAGNOSTIC AND TROUBLESHOOTING AIDS

2.1 INTRODUCTION

This chapter contains troubleshooting information, diagnostic error message interpretation, and module configuration information.

NOTE

The UNIBUS powerup protocol on PDP-11/84 systems is slightly different from other PDP-11 systems.

With other PDP-11 systems, UNIBUS signal INIT L is held asserted for a minimum of 10 ms after the negation of DCLO L.

On PDP-11/84 systems, UNIBUS signal INIT L is held asserted for a minimum of 16 ms after the negation of DCLO L. This difference will not affect any system operations.

2.2 GENERAL TROUBLESHOOTING NOTES

1. The corrective maintenance strategy is field replaceable unit (FRU) replacement.
2. As a quick power check, check the cabinet blower or the box fans for operation.
3. Verify the symptoms reported by the customer before removing any components.
4. The troubleshooting information in this guide assumes that only one FRU has failed.
5. Check system cables for loose connections and any damaged cables or wires. Replace if necessary.
6. Spare FRUs may be dead-on-arrival (DOA); do not ignore the possibility that a newly installed FRU is faulty.
7. Symptoms displayed on the console terminal or LEDs can indicate multiple failures; therefore, the symptoms may change as FRUs are replaced. Always troubleshoot the current symptoms.

2.3 DIAGNOSTIC TYPES

PDP-11/84 A- and P-series systems support three types of diagnostic programs.

1. DECX11 – provides system tests to check the interaction of each option and isolate system failures to the subsystem component.

2. XXDP+ – provides tests that check individual options and local- ize hardware failures to the function level.

3. Read Only Memory (ROM) resident – CPU ROM-resident startup diagnostics test various functions specific to the system modules and private memory interconnect (PMI) bus, and isolate failures to the module or option level.

The following A- and P-series XXDP+ diagnostic programs test various functions on the three kernel modules. To initiate an XXDP+ diagnostic, the system must first successfully complete the startup diagnostics.

A-Series Diagnostics:

OKDA?? (KDJ11-BF)

OKTA?? (KTJ11-B)

VMJA?? (MSV11-J)

P-Series Diagnostics:

OKDA?? (KDJ11-BC)

OKTA?? (KTJ11-B)

VMSA?? (MSV11-R)

The "??" at the end of the diagnostic names ensures that the latest diagnostic version is executed when called.

To load and execute any diagnostic issue, the RUN command followed by the diagnostic name. For example:

. R OKDA?? <CR>

The startup diagnostics are executed during a system power-up or restart. A failure during diagnostic execution halts the testing and displays one of the following.

1. An error code and an error message on the console terminal (if connected).

2. An error code on the front panel STARTUP TEST display.

3. The error code in the CPU module diagnostic LEDs.

Normally, the system displays the same error information in all three locations. If the console terminal is not working, refer to the STARTUP TEST display. If neither location is working, refer to the CPU module LEDs.

2.4 CONSOLE TERMINAL ERROR MESSAGE FORMAT

A typical console error message is shown in Figure 2-1.

```
Testing in progress - Please wait
Memory Size is 1024 K Bytes
9 Step memory test
  Step 1 2 3 4 5 6 7 8

Error 46
Memory CSR Error

See troubleshooting documentation

Error PC= 173436  PCR page= 15   Program listing address= 015436

R0 = 060000     R1 = 052525     R2 = 172100     R3 = 172344
R4 = 100000     R5 = 040000     R6 = 172300     Par3 = 010000

Command    Description

   1       Rerun test
   2       Loop on test
   3       Map memory and I/O page

Type a command then press the RETURN key:
```

Figure 2-1 Error Message Display Example

2.4.1 Console Error Message Description

The console error message contains the following information:

1. An error code – This is the octal number of the startup diagnostic test that failed.

   Table 2-1 lists the error codes, test descriptions, and probable causes.

2. An error description – This is a one-line description of the error.

   Table 2-2 lists the error messages and their descriptions.

3. A "See troubleshooting documentation" message.

4. Error address line – This address line specifies the error program counter (Error PC=), the page number in the ROM (PCR page=), and the address to reference in the program listing (program listing address=).

   In the case of unexpected traps, the error address is the address following the instruction that caused the unexpected trap.

5. The content of R0–R6 of register set 0, and the content of kernel page address register (PAR) 3. The tests do not use register set 1. Register set 1 is used mainly by ROM code support routines.

6. For some tests the system displays the failing address, the expected data, and the received data (bad data).

7. A command line that describes user-selectable commands. To execute a command, enter the associated command number (e.g., **1**, **2**, etc.) and press the **Return** key. The commands are:

   a. **1** followed by the **Return** key – rerun the test. If the test passes the ROM code will continue testing. If all other tests pass, the ROM code will display the total number of errors and enter dialog mode regardless of the mode selection in the electronically erasable programmable read-only memory (EEPROM).

   b. **2** followed by the **Return** key – loop on test. This option causes the ROM code to continuously loop on the test that failed. These loops are generally very large and are not intended to be used as scope loops.

      The test runs until an error occurs or end-of-test has been reached. In either case, the test is started again and continues to loop until the user types **<CTRL/C>** at the console. At this point, the ROM code will display the total number of errors and the total number of successful passes if any.

      Both the error counter and the pass counter have a maximum value of 65535. If either counter reaches this value the count will not overflow to zero; it will stay at this value.

   c. **3** followed by the **Return** key – map memory and I/O page. This command is normally used if a memory error occurs. If a memory is not configured properly the MAP command may point to where the memory actually is.

      In a multi-memory system in which one memory fails, this command can be used as a method of physically identifying the failing memory, if it has a communications status register (CSR).

      This command is only available when the bus is turned on. The command is not available for tests (or codes) 76 through 56.

   d. **4** followed by the **Return** key – advance to the next test. This command allows the user to bypass the failing test and continue. This command will only show up for errors that are generally considered nonfatal.

      If the error is fatal and Field Service would like to bypass the error, it is possible by typing **<CTRL/O>**, **4** and the **Return** key, and the command will be executed.

CAUTION

Errors should not be bypassed unless all user software has been removed or write-protected.

At this point, the ROM code flushes its input buffer of any previously typed characters and waits for input from the user.

Table 2-1 Error Codes, Test Descriptions, and Probable Causes

Error Code	Test Description	Probable Cause
77	Initially set to this value on power-up.	The halt switch is on at power-up. A UNIBUS bus grant (BGn) or nonprocessor grant (NPG) line is open and slave acknowledge (SACK) is being asserted by the bus. Check monitor and distribution module (MDM). All grant cards must be installed. Terminator is faulty. Power supply is faulty.
76	First CPU tests, memory management unit (MMU) register tests.	M8190
75	Turn MMU on. Run MMU and CPU tests.	M8190
74	Turn on private memory interconnect (PMI) and look at the UNIBUS adapter (UBA) RESTART bit. Then turn off PMI.	M8190, M8191
73	Power-up to octal debugging technique (ODT).	Not a failure – selected mode is ODT in EEPROM and the system is in (J11) ODT.
72	Power-up to 24/26.	M8190, M8191
71	EEPROM checksum tests.	EEPROM accidentally written; restore data using setup mode commands; verify W40 installed on M8190 module.
70	CPU ROM checksum and PC tests.	M8190
67	Miscellaneous CPU and extended instruction set (EIS) tests.	M8190
66	Console serial line unit (SLU) test 1 – check for each register's response.	M8190
65	Console SLU test 2 – transmit and receive data in maintenance mode.	M8190
64	Console SLU test 3 – check interrupts and errors in maintenance mode.	M8190
63	Test MMU aborts.	M8190
62	Standalone mode CPU cache tests.	M8190
61	Clock test.	M8190 Clock from power supply.
60	Floating-point processor.	M8190
57	Unused.	

Table 2-1 Error Codes, Test Descriptions, and Probable Causes (Cont.)

Error Code	Test Description	Probable Cause
56	Exit standalone mode. Check location of address 17 760 000 for timeout.	M8191 M8190
55	UBA register response test, check UNIBUS through diagnostic data register (DDR) for hung lines.	M8191 UNIBUS failure M8190
54	Memory size test.	UNIBUS failure
53	Check memory present at location 0.	PMI memory
52	0 - 4K word memory test.	PMI memory, M8190
51	Cache testing using PMI memory.	M8190
50	Memory test 1 - data tests byte tests.	PMI memory
47	Memory parity/error correction code (ECC) tests.	PMI memory
46	Memory address/shorts test.	PMI memory
45	UBA ROM response test.	M8191
44	UBA map registers data path test.	M8191
43	UBA unmapped diagnostic cycles test.	M8191
42	UBA mapped diagnostic cycles test.	M8191
41	UBA floating address/data test using mapped diagnostic cycles.	M8191
40	UBA address overflow test.	M8191
37	UBA cache data test.	M8191 PMI memory
36	UBA cache least recently used (LRU) test.	M8191
35	UBA cache floating address test in tag store.	M8191
34	UBA cache parity error detection test.	M8191
33	UNIBUS memory data path test.	UNIBUS memory M8191
32	UNIBUS memory parity logic test.	UNIBUS memory
31	UNIBUS memory address/ shorts test.	UNIBUS memory

Table 2-1 Error Codes, Test Descriptions, and Probable Causes (Cont.)

Error Code	Test Description	Probable Cause
	NOTE **With the exception of error codes 25, 22, and 6, codes 30 through 1 are bootstrap problem indicators and are not diagnostic errors.** **Some may be corrected by the user. Others may be indicators of errors in the device being bootstrapped.**	
30	Test exit routine.	
27	Unused.	
26	Unused.	
25	Air movers and voltage regulator test.	Cabinet blower Box fans H7213 regulator module Minimum load module (MLM) not installed. No memory module(s) in system.
	NOTE **Error code 25 is not used in P-series systems.**	
24	Unused.	
23	XON not received after XOFF. To correct, type **<CTRL/Q>** at the console.	Console terminal not ready due to XOFF signal received from terminal while attempting to print a message. This is normally not considered a failure, because the condition could be operator error (if the operator has typed **<CTRL/S>** without following with **<CTRL/Q>**, the terminal is not ready, out of paper, etc.).
22	Console SLU transmit ready bit not set.	M8190
21	Drive error.	The device that the user is attempting to boot is displaying an error code in its error register. Verify that media is in good condition and bootable.
20	Controller error.	The UNIBUS controller for the device the customer is attempting to boot is displaying an error code in its CSR. Ensure that the NPG jumper was removed if the device is a direct memory access (DMA) controller. Consult the device's technical manual for more information.

Table 2-1 Error Codes, Test Descriptions, and Probable Causes (Cont.)

Error Code	Test Description	Probable Cause
17	Invalid device.	The mnemonic typed in for the boot device is either incorrect or the boot ROM for that device is not installed. Go to the dialog mode and "LIST" the valid devices.
16	Invalid unit number.	The unit number after the mnemonic is not within acceptable range for that device. See that device's technical manual for help.
15	Nonexistent drive.	The drive number the user is trying to boot from is not on the PDP-11/84.
14	Nonexistent controller.	The controller for the device the user is trying to to boot from is not on the UNIBUS or is addressed incorrectly.
13	No tape present.	No tape installed.
12	No disk present or drive is not loaded correctly.	No media in drive or the drive LOAD button not in.
11	Nonbootable media is in the drive.	The bootstrap data from the device does not conform to the boot block specifications. Ensure that media is bootable. Change setup mode to accept nonstandard boot blocks.
10	Drive not ready.	No media present in the drive or the disk drive has not completed its spinup function.
6	Console disabled.	Self explanatory.
5	Unused.	
4	Dialog mode.	The system is in dialog mode and waiting for input from the console terminal to rewind.
3	UBA ROM boot in progress.	May take a few seconds.
2	EEPROM boot in progress.	May take a few seconds.
1	CPU ROM boot in progress.	May take up to 5 minutes for some devices.
Blank		Program control has been transferred to a secondary boot, an EEPROM boot, or a UBA/M9312 boot.

Table 2-2 Startup Diagnostic Error Message Descriptions

Error Message	Description
M8190 CPU Cache Error	CPU cache logic error
M8190 FP Error	CPU floating-point error
M8190 CPU ROM Error	CPU ROM logic or checksum error
M8190 EEPROM Checksum Error	CPU EEPROM logic or checksum error
M8190 Clock Error	CPU clock logic or power supply clock error
M8190 CPU Error	Other CPU errors
UNIBUS Signal Error	A UNIBUS signal is always asserted
No memory in location 0	Memory failed or is addressed incorrectly
Memory Error	General memory test errors
Memory CSR Error	Memory errors during parity or ECC testing
M8191 UBA Cache Error	UBA cache error
M8191 UBA Error	Other UBA errors
Unexpected trap to location	This is a general error message that occurs during any unexpected traps. The address of the trap follows this message.

2.4.2 Unexpected Trap and MMU Error Code Descriptions

Figure 2-2 shows an example of the error code and message displayed when an unexpected trap occurs. The error number of unexpected traps is always the current test number plus 100.

NOTE
Operator input is underlined in the following examples.

In the example, the error code (or test number) is 62. The actual error code is read as 162. The STARTUP TEST display will display 62 since it is only a two-digit display.

Unexpected traps are always considered fatal errors.

```
Testing in progress - Please wait

Error 162
Unexpected trap to location 250 MMU

See troubleshooting documentation


Updated PC= 173436  PCR page= 15 Program listing address= 015436

R0 = 101365     R1 = 076410     R2 = 177746     R3 = 177744
R4 = 101367     R5 = 000250     R6 = 172276     Par3 = 052400

Command    Description

   1       Rerun test
   2       Loop on test


Type a command then press the RETURN key:
```

Figure 2-2 Unexpected Trap Error Example

For codes 76 and 75, the ROM code displays the single letter E followed by the test number (Figure 2-3). After the message is displayed, the ROM code will not accept any input. The only option for the user is to restart the system or repair the problem.

```
E 76
```

Figure 2-3 Example of Test Error

2.4.3 Boot Program Error Codes/Messages

Error codes 21 through 10 (described in Table 2-1) are associated with the boot programs for disks, tapes, and DECnet devices. These errors are applicable for all CPU ROM-resident boot programs, and any EEPROM boots that are written to pass these errors back to the CPU ROM. Only errors 14, 16, and 17 apply to UBA or M9312-type ROM boots.

Figures 2-4 and 2-5 show examples of an error from a boot program when the BOOT command is used in dialog mode.

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key: B DL1 <CR>

Trying DL1

Message 12
No disk present, or drive is not loaded correctly

Command    Description

1       Reboot
2       Go to Dialog mode

Type a command then press the RETURN key:
```

Figure 2-4 Boot Program Error Example

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key: B DL3 <CR>

Trying DL3


Message 15
Non existent drive

Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key:
```

Figure 2-5 Boot Error Message Example

When the ROM code enters the automatic boot sequence, all boot error messages are suppressed on the first pass through the list of boot devices. If no device is successfully booted on the first pass, the ROM code will restart the automatic boot sequence and try to boot all of the selected devices again and display all applicable error messages.

When the ROM code has failed to boot any of the devices selected in the automatic boot list, dialog mode is entered. Figure 2-6 shows an example of a boot error display when the automatic boot sequence failed to find a bootable device and dialog mode is entered.

```
Testing in progress - Please wait
Memory Size is 1024 K Bytes
9 Step memory test
Step 1 2 3 4 5 6 7 8 9

Starting automatic boot

Trying DU0      No disk present, or drive is not loaded
Trying DU1      Non bootable media in the drive
Trying DU2      Drive not ready
Trying DU3      Drive Error
Trying DL0      No disk present, or drive is not loaded


Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key:
```

Figure 2-6 Automatic Boot Error Message Example

2.5 SYSTEM TROUBLESHOOTING AIDS

The system provides the following troubleshooting aids.

1. LED monitors.
2. Voltage test points.
3. Monitor logic with audible alarm.

2.5.1 Front Panel

The front panel indicator DC ON monitors the dc output voltages on the main power supply (Figure 2-7).

If the DC ON LED is off, the probable cause is one of the power supply regulators. Each regulator has a specific LED monitor located on the MDM module.

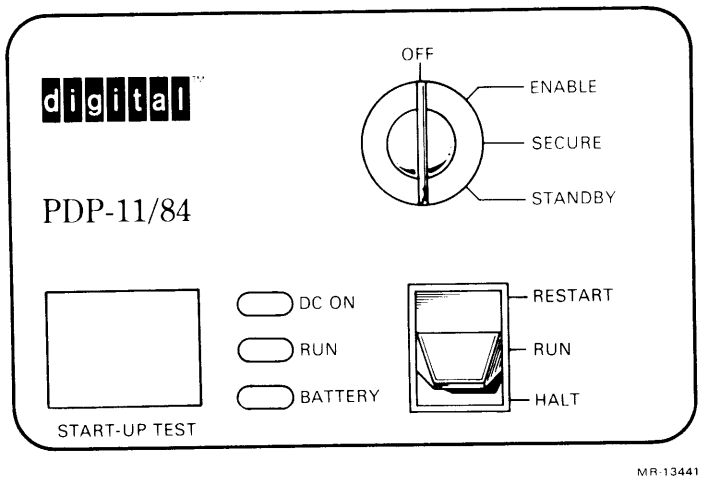

Figure 2-7 System Front Panel

2.5.2 MDM Module

The MDM module provides the following troubleshooting aids.

1. LEDs that monitor most power supply voltages (Figure 2-8).
2. Test points for checking the main power supply voltages.
3. Blower/fan rotation monitoring logic.

The tolerance for each voltage should be within ± 10%, checked on the test points located above the LEDs. If a voltage is found to be out of tolerance or not present, one of the power supply regulators specified in Table 2-3 is the probable fault.

The rotation monitor logic indirectly checks the +12 Vdc. If the blower/fans fail to send a rotation-based pulse, the monitor logic causes an audible alarm to sound and powers down the system one minute later.

Table 2-3 Power Supply Regulator Fault Isolation

LED	Voltage(s) Monitored	Probable Cause
D1	+5 V main power supply	H7200 in H7202-KA
D2	+5 VBB and +12 V blower/fan	H7213 in H7202-KA
D3	±15 V main power supply	H7211 in H7202-KA
D4	+5 V expansion power supply	H7200 in H7202-KB
D5	±15 V expansion power supply	H7211 in H7202-KB

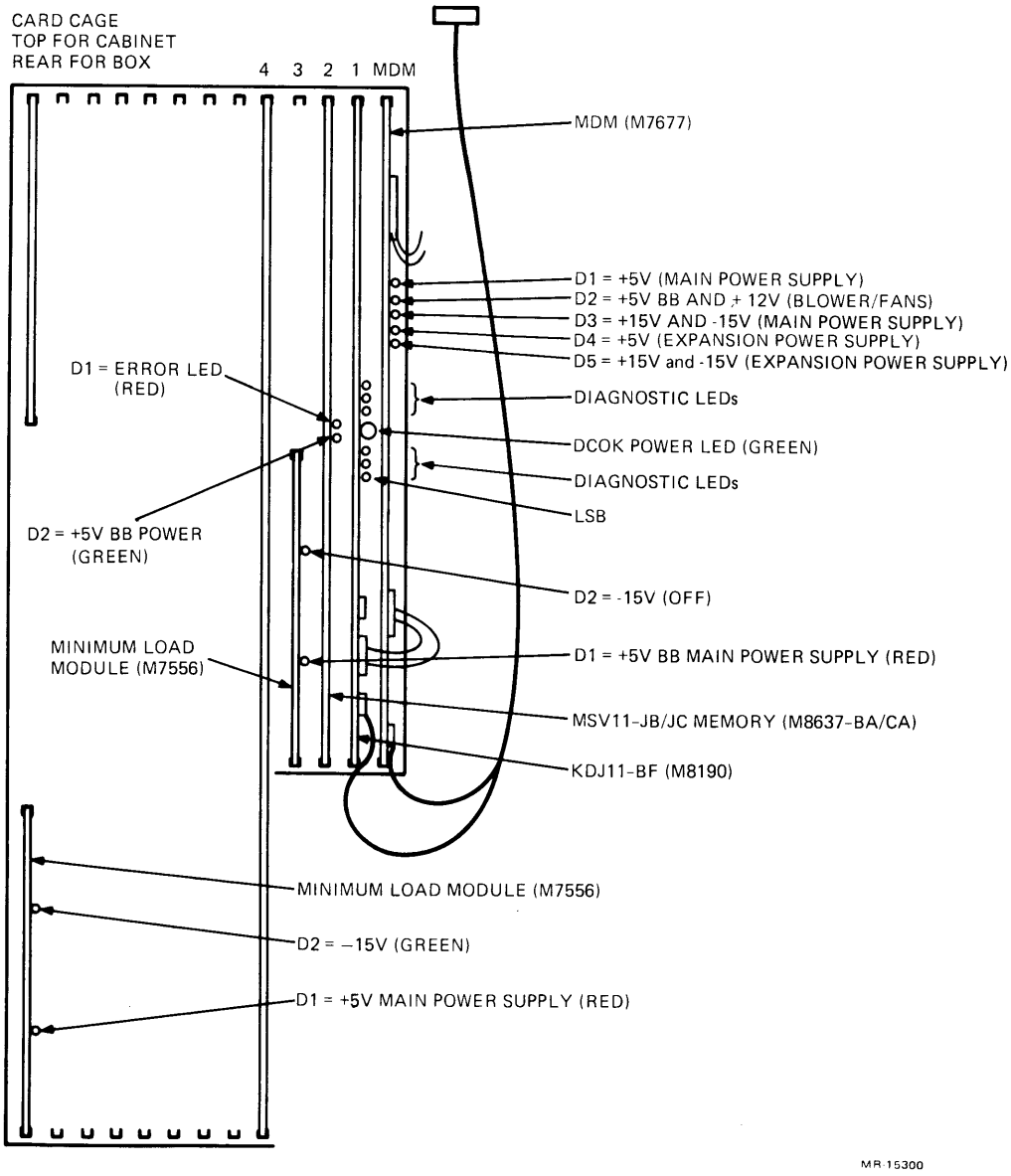

Figure 2-8 MDM Module LED Layout

MDM Module Notes:

1. An M7677-YA MDM must be used if the system contains an H7231-E or -F BBU.
2. If the MDM is the suspected problem, check the voltage test points and the NPG switch pack configuration prior to module replacement (Figure 2-9).
3. Loss of voltage turns off the associated LED.
4. If an LED indicates loss of voltage, check the corresponding test point prior to regulator replacement.

5. The setting of the NPG select switch pack is used to select NPG status. Each NPG switch corresponds to a CPU backplane slot 5 through 12. Figure 2-9 shows the location and slot number of the each NPG switch.

6. For non-DMA devices, the NPG switch should be in the ON position. A common NPG problem occurs when DMA devices are installed with the NPG switch ON (arbitration mechanism is bypassed).

   This causes an error code 20 when attempting to boot that device, indicating a controller error. To correct the problem, turn off the NPG switch for that slot.

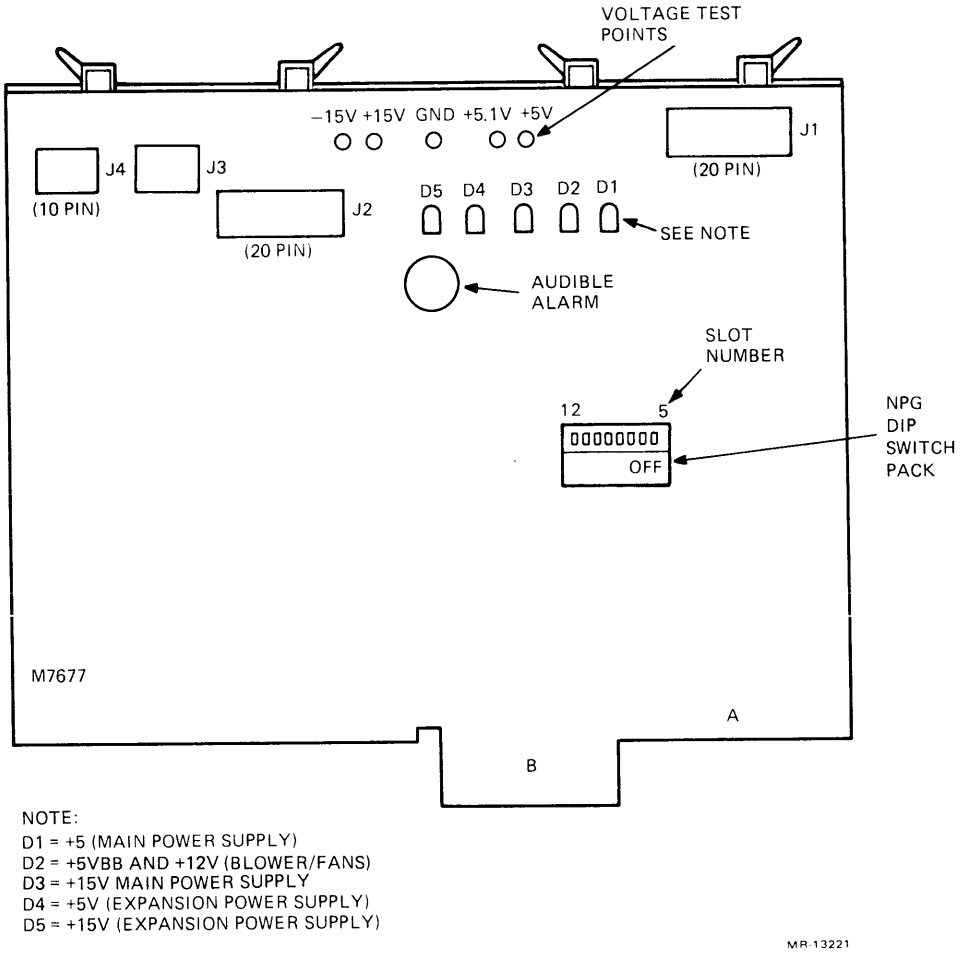

Figure 2-9 MDM Module Layout

2.5.3 KDJ11-BF/BC CPU Module

The KDJ11-BF/BC module provides the following.

1. A green power OK (POK) LED, indicating that dc power to the CPU module is present.
2. Six red error code LEDs, which correspond to the startup diagnostic error codes (Figure 2-10).

If the CPU module is the suspected problem, check the following prior to module replacement.

1. The module jumper configurations are as specified in Figure 2-10.
2. The dual in-line package (DIP) switches are off.

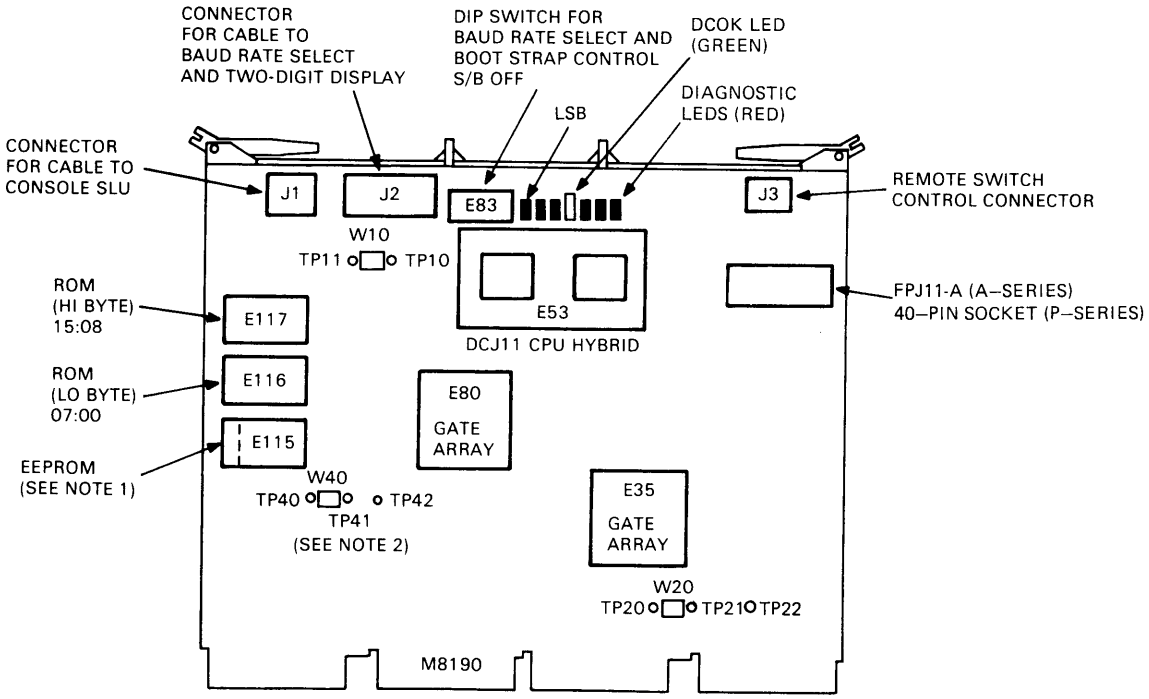

Figure 2-10 KDJ11-BF/BC Jumper and Switch Pack Locations

2.5.4 MSV11-JB/JC Memory Module

The quad-height memory module provides the following.

1. A red LED to indicate uncorrectable errors
2. A green LED to indicate the presence of +5 Vdc
3. Two switch packs for starting and CSR address selection
4. Four factory-set jumpers.

If the module is the suspected problem, check both LEDs, the switch pack settings, and jumper configurations prior to module replacement. See Figure 2-11 for LED, switch pack, and jumper layout.

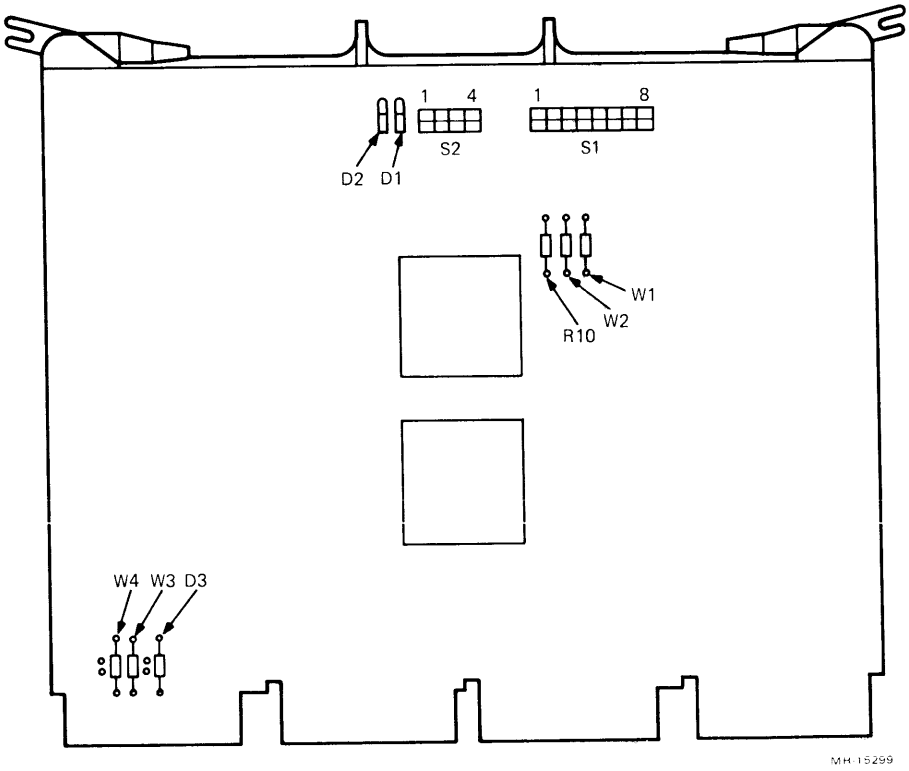

Figure 2-11 MSV11-JB/JC LED/Switch Pack/Jumper Layout

NOTE

Do not run the XXDP+ diagnostic if the module fails the startup diagnostic test. The startup diagnostic tests most of the memory module functions thoroughly. The XXDP+ diagnostic requires between 20 and 60 minutes to complete.

The starting address is configured using switch pack S1, switches 1 – 8. Table 2-4 lists the switch settings, starting addresses, and decimal numbers. The top 16 entries apply to the 1 Mbyte (MSV11-JB) memory and the bottom 16 entries apply to the 2 Mbyte (MSV11-JC) memory.

Table 2-4 MSV11-JB/JC Starting Address

Switch Setting * 1 2 3 4 5 6 7 8	Starting Address (Octal)	Decimal (K)
0 0 0 0 0 0 0 0	00 000 000	0
0 0 0 0 0 0 0 1	00 040 000	8
0 0 0 0 0 0 1 0	00 100 000	16
0 0 0 0 0 0 1 1	00 140 000	24
0 0 0 0 0 1 0 0	02 000 000	32
0 0 0 0 0 1 0 1	00 240 000	40
0 0 0 0 0 1 1 0	00 300 000	48
0 0 0 0 0 1 1 1	00 340 000	56
0 0 0 0 1 0 0 0	00 400 000	64
0 0 0 0 1 0 0 1	00 440 000	72
0 0 0 0 1 0 1 0	00 500 000	80
0 0 0 0 1 0 1 1	00 540 000	88
0 0 0 0 1 1 0 0	00 600 000	96
0 0 0 0 1 1 0 1	00 640 000	104
0 0 0 0 1 1 1 0	00 700 000	112
0 0 0 0 1 1 1 1	00 740 000	120
0 0 0 0 X X X X	00 000 000 – 00 740 000	000 – 120
0 0 0 1 X X X X	00 100 000 – 01 740 000	128 – 248
0 0 1 0 X X X X	02 000 000 – 02 740 000	256 – 376
0 0 1 1 X X X X	03 000 000 – 03 740 000	384 – 504
0 1 0 0 X X X X	04 000 000 – 04 740 000	512 – 632
0 1 0 1 X X X X	05 000 000 – 05 740 000	640 – 760
0 1 1 0 X X X X	06 000 000 – 06 740 000	768 – 888
0 1 1 1 X X X X	07 000 000 – 07 740 000	896 – 1016
1 0 0 0 X X X X	10 000 000 – 10 740 000	1024 – 1144
1 0 0 1 X X X X	11 000 000 – 11 740 000	1152 – 1272
1 0 1 0 X X X X	12 000 000 – 12 740 000	1280 – 1400
1 0 1 1 X X X X	13 000 000 – 13 740 000	1408 – 1528
1 1 0 0 X X X X	14 000 000 – 14 740 000	1536 – 1656
1 1 0 1 X X X X	15 000 000 – 15 740 000	1664 – 1784
1 1 1 0 X X X X	16 000 000 – 16 740 000	1792 – 1912
1 1 1 1 X X X X	17 000 000 – 17 740 000	1920 – 2040

* 1 = Switch on
0 = Switch off
X = Switch can be either on or off

The CSR address is configured using switch pack S2, switches 1 – 4. The base address is 17772100. Each successive address is the base plus 2. Table 2-5 lists all 16 possible CSR addresses.

Table 2-5 MSV11-JB/JC CSR Address Selections

S2 Setting 1 2 3 4	CSR Address (Octal)
0 0 0 0	17 772 100
0 0 0 1	17 772 102
0 0 1 0	17 772 104
0 0 1 1	17 772 106
0 1 0 0	17 772 110
0 1 0 1	17 772 112
0 1 1 0	17 772 114
0 1 1 1	17 772 116
1 0 0 0	17 772 120
1 0 0 1	17 772 122
1 0 1 0	17 772 124
1 0 1 1	17 772 126
1 1 0 0	17 772 130
1 1 0 1	17 772 132
1 1 1 0	17 772 134
1 1 1 1	17 772 136

The jumper configurations for the MSV11-JB and MSV11-JC memory modules are different. Ensure that the factory-set jumpers are as specified in Table 2-6.

Table 2-6 MSV11-JB/JC Jumper Configurations

Module	Jumper(s)	Position	Description
MSV11-JB			
	W1	Out	256K Dynamic RAMs
	W2	In	Half-populated module
	W3,W4	Vertical	Reserved for future use
MSV11-JC			
	W1	Out	256K Dynamic RAMS
	W2	Out	Fully populated module
	W3,W4	Vertical	Reserved for future use

2.5.5 MSV11-R Memory Module

The quad-height memory module provides the following.

1. A red LED for monitoring parity errors
2. A switch pack for memory starting address and CSR address selection

Figure 2-12 shows the location of the switch pack and LED. If the module is the suspected problem, check the parity LED and switch pack settings before module replacement.

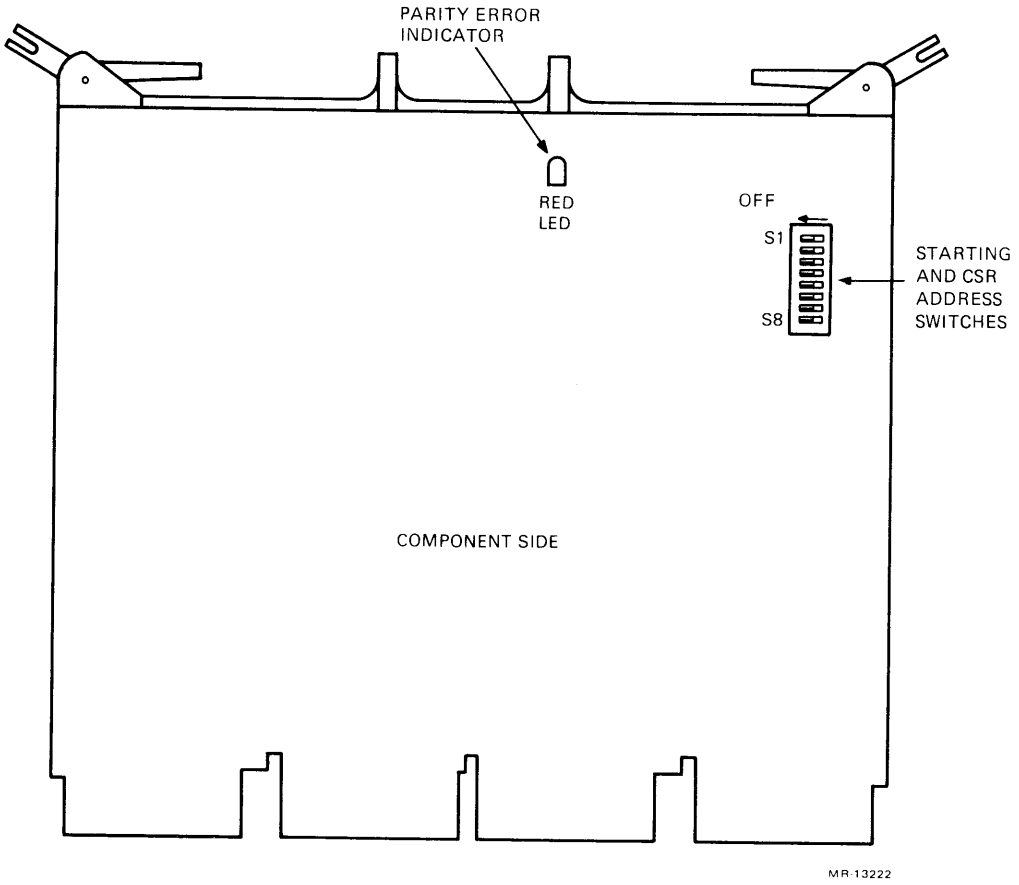

Figure 2-12 MSV11-R Switch Pack and LED Locations

NOTE

1. **Do not run the XXDP+ diagnostic if this module fails the startup diagnostic test. The startup diagnostic checks most of the memory functions thoroughly. The XXDP+ diagnostic requires approximately 40 minutes to complete.**

2. **Switches S3 and S4 of the switch pack should always be in the OFF position.**

Switches S1 and S2 of the switch pack configure the starting address. They enable the starting address on 1 Mbyte boundaries. See Table 2-7 for S1 and S2 settings.

Table 2-7 MSV11-R Starting Address Selection

S1	S2	Starting Address
OFF	OFF	00 000 000
OFF	ON	04 000 000
ON	OFF	10 000 000
ON	ON	14 000 000

Switches S5 through S8 on the switch pack configure the CSR address. The base CSR address is 17 772 100. Each successive address is the base plus 2. See Table 2-8 for the starting address for all 16 possible starting addresses.

Table 2-8 MSV11-R CSR Address Selection

S5	S6	S7	S8	CSR Address
ON	ON	ON	ON	17 772 100
ON	ON	ON	OFF	17 772 102
ON	ON	OFF	ON	17 772 104
ON	ON	OFF	OFF	17 772 106
ON	OFF	ON	ON	17 772 110
ON	OFF	ON	OFF	17 772 112
ON	OFF	OFF	ON	17 772 114
ON	OFF	OFF	OFF	17 772 116
OFF	ON	ON	ON	17 772 120
OFF	ON	ON	OFF	17 772 122
OFF	ON	OFF	ON	17 772 124
OFF	ON	OFF	OFF	17 772 126
OFF	OFF	ON	ON	17 772 130
OFF	OFF	ON	OFF	17 772 132
OFF	OFF	OFF	ON	17 772 134
OFF	OFF	OFF	OFF	17 772 136

2.5.6 KTJ11-B Module

The module provides four sockets to support M9312 compatible ROMs. If this module is the suspected problem, check the ROMs and their orientation as shown in Figure 2-13.

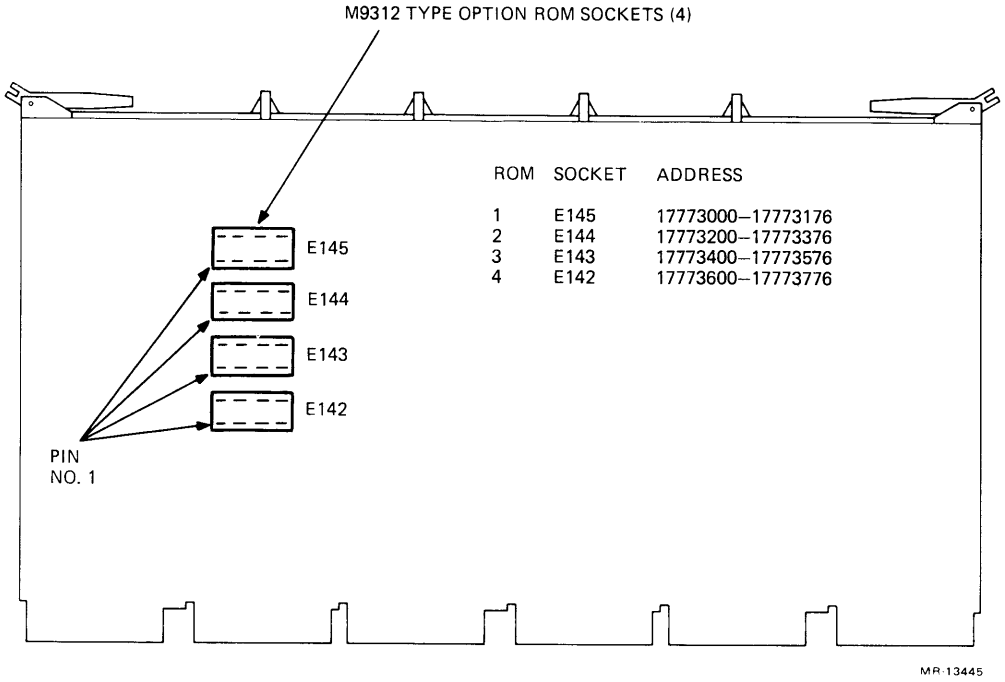

Figure 2-13 KTJ11-B ROM Socket Locations

2.5.7 Minimum Load Module

The MLM modules are used to provide minimum power supply regulator loads under the following conditions.

1. If only one memory module slot is occupied, an MLM is inserted in CPU backplane slot 3 (rows C and D) to ensure a minimum current drain of 2 A from the +5 VBB regulator.
2. An MLM is inserted in CPU backplane slot 12 (rows E and F) to ensure a minimum current drain of 1 A from the −15 Vdc regulator.
3. If an expansion backplane (DD11-CK or DD11-DK) is installed, an MLM is inserted in the last slot of the backplane (rows E and F) to ensure a minimum current drain of 1 A from the −15 Vdc regulator.

NOTE

An MLM is not required in the last backplane slot (CPU or expansion) if the installed options draw the minimum current drain of 1 A of −15 V.

An MLM module in an expansion backplane only monitors the −15 Vdc.

When not required, the load modules must be removed from the backplane.

As shown in Figure 2-14, the MLM has two LEDs to indicate the presence of +5 VBB (RED, D1) and −15 Vdc (GREEN, D2).

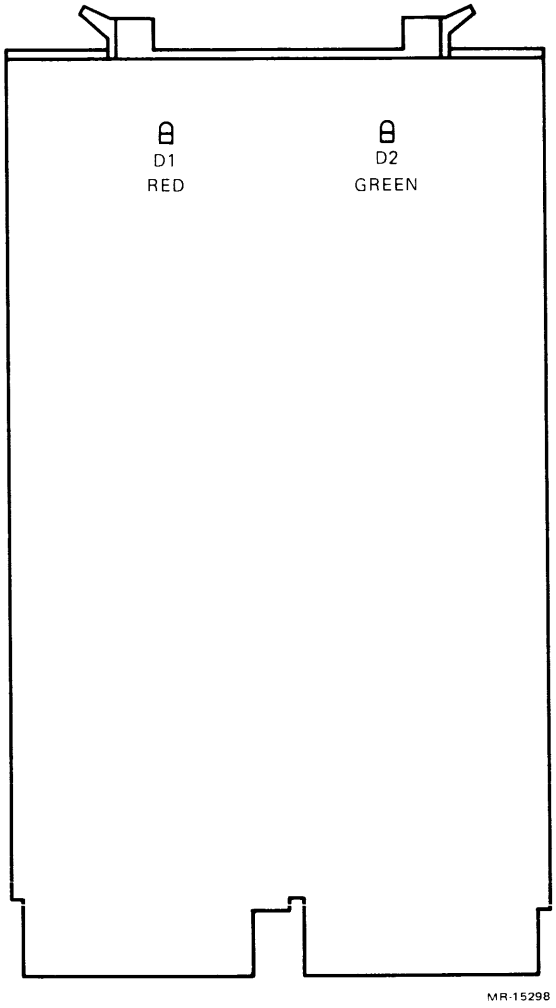

Figure 2-14 Minimum Load Module Layout

2.6 J11 MICRO ODT

J11 Micro ODT (ODT) is entered anytime the CPU is halted by one of the following.

1. Placing the front panel toggle switch in the HALT position
2. Executing a halt instruction, if the halt mode is enabled and the system is in kernel
3. Pressing the **Break** key, if the terminal is set up to generate a break character, and the front panel keylock switch is set to ENABLE.

Table 2-9 summarizes the ODT commands. The figures following the table provide examples for most of the commands. Note that operator input is underlined.

Table 2-9 J11 Micro ODT Command Summary

Command	Symbol	Description
Slash	n/	Opens and outputs the contents of a memory location, I/O device register, internal processor register, or processor status (PS) register. The / must be preceeded by octal digits (n) to specify the register or location. See Figure 2-15 for example.
Carriage return	<CR>	Closes an open location. If a location's contents are to be changed, precede the <CR> with the new data. If no change is desired, <CR> closes the location without altering its content. See Figure 2-15 for example.
Line feed	<LF>	Closes an open location and opens the next contiguous location. Memory addresses are incremented by two, and processor registers are incremented by one. If the PS is opened, it is closed and no new location is opened. See Figure 2-16 for example.
Internal register	$n or Rn	Either character - when followed by a register number 0 to 7, or the PS designator (S) - will open the specified processor register. If more than one number is entered after R or $, the last number entered will be used.
Processor status word designator	S	Opens the processor status register. The designator must follow $ or R.
Go	G	Starts program execution at the location entered immediately before the G. If G is issued with the front panel switch set to HALT, the system is initialized, ODT re-entered, and the PC displayed. G truncates the address entered in the last 16 bits. For example, 7 777 773 000G would be read as 173 000G. Since memory management is disabled by G, the starting address is always in the lower 28K of memory or the I/O page. See Figure 2-17 for example.
Proceed	P	Resumes program execution. The command corresponds to CONTINUE on other PDP-11 consoles. Program execution resumes at the address pointed to by the PC. If P is issued with the front panel switch set to HALT, it is recognized at the end of instruction execution, ODT is re-entered, and the PC displayed. The user can thus single-instruction step through a program and obtain a PC trace on the console terminal. See Figure 2-18 for example.
Binary dump	<Ctrl/ Shift/S>	Manufacturing use only. It is not recommended this command be used.

2.6.1 ODT Notes

1. When entering addresses or data, leading zeros are not required. They will be filled by ODT.
2. When entering addresses in the I/O page, all 22 bits must be entered (e.g., 17 776 100).
3. A ? (question mark) will be printed whenever illegal characters are entered, addresses are accessed that result in a timeout, or a parity error is detected.

2.6.2 ODT Command Examples

```
@1000/ 012737 <CR>          ;Open memory location 00001000.
                            ;The contents (012737) are
                            ;displayed. <CR> closes the
                            ;location without modification.

@100/ 000200 7422 <CR>      ;Open memory location 00000100
                            ;and deposit data (7422) and
                            ;close the location.

@/ 007422 6422 <CR>         ;Re-open the location and deposit
                            ;new data.
```

Figure 2-15 / (Slash) Command Example

```
@1000/ 012737 <LF>          ;Location 1000 is opened, the
                            ;contents are displayed, and
                            ;then closed with <LF>.

00001002 100200 0 <LF>      ;The <LF> caused the next
                            ;location to be opened and the
                            ;contents to be displayed. In
                            ;this case the contents are
                            ;changed the operator.

00001004 176100 <CR>        ;The next location is opened
                            ;to examine the contents and
                            ;then closed with <CR>.
```

Figure 2-16 LINE FEED Command Example

```
@1000G      ;The program is started at location 1000.

@1000G      ;The program is started with the Halt switch
            ;on. The CPU initializes registers and then
            ;halts without executing the first instruction.
@1000       ;The PC is displayed and then the ODT prompt
            ;is displayed.
```

Figure 2-17 GO Command Example

```
@R7/002464 1000 <CR>        ;R7 (PC) is opened and the
                            ;contents displayed. The new
                            ;address is entered in R7.
@P                          ;The proceed command is issued
                            ;and the program continues at
                            ;location 1000.

@P                          ;The proceed command is issued
                            ;with front panel switch in the
001004                      ;Halt position. The PC is
                            ;displayed.
@P                          ;
                            ;Etc.
001010                      ;
@                           ;
```

Figure 2-18 PROCEED Command Example

2.7 DIALOG MODE COMMAND DESCRIPTIONS

When dialog mode is entered, the ROM program prints out the message shown in Figure 2-19 at the console terminal and waits for the user to select a command.

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key:
```

Figure 2-19 Dialog Mode Commands

Dialog mode command notes:

1. The user may obtain a brief description of each command by typing **H** followed by pressing the **Return** key or by typing **?** only.

2. All commands may be executed by typing only the first letter of the command followed by the **Return** key. For example, the MAP command can be invoked by typing **M** or **MA** or **MAP**.

3. On command input, all lower-case letters are converted to upper-case, and leading spaces and tabs are ignored.

4. If the terminal type selection in the EEPROM is video, the ROM code will erase the previous character on the screen when the **Delete** key is pressed. If the terminal type is hard copy, the ROM code will use slashes (/) to identify all deleted characters.

5. Use **<CTRL/U>** at any time to delete the entire command line. **<CTRL/U>** is not echoed by the ROM code.

6. **<CTRL/R>** will retype the command line. **<CTRL/R>** is normally used when the terminal type is hard copy to clear up command lines where the **Delete** key has been used. **<CTRL/R>** is not echoed by the ROM code.

7. Input is limited to 16 characters and spaces. If more than 16 characters are entered, the ROM code will delete all input and retype the KDJ11-B prompt. Typing the seventeenth character is equivalent to typing **<CTRL/U>**.

8. The ROM code will ignore any space or tab typed prior to a character, or the second tab or space typed in a row without a printable character in-between. All tabs are converted to and echoed as spaces.

9. If an invalid input is received an "invalid entry" message will be typed and the header prompt repeated.

10. In some cases the following command examples may not represent the exact printout or screen display.

NOTE

If additional information is required for any dialog mode command refer to Chapter 4 of the *PDP-11/84 System Installation and Technical Reference Manual.*

The following subsections summarize each command and provide execution examples.

2.7.1 HELP Command

The HELP command prints out a brief description of all available commands (Figure 2-20). It can be executed by typing **H** and the **Return** key, or typing **?** only. Dialog mode is restarted at the end of the command.

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key: H <CR>

Command     Description

Help        Type this message
Boot        Load and start a program from a device
List        List boot programs

Setup       Enter Setup mode
Map         Map memory and I/O page
Test        Continuous self test - Type <CTRL/C> to exit

Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key:
```

Figure 2-20 HELP Command Display

2.7.2 BOOT Command

The BOOT command initiates a device bootstrap (Figure 2-21). Command arguments are the device name and the unit number. If the device name is left off, the program prompts for it. If the unit number is left off, the program assumes unit zero. The unit number ranges from 0 to 255(10) depending on the device and the boot program.

These are the three optional switches used with the BOOT command.

/A Request to allow the user to type in a nonstandard CSR address for the controller.

/O The unit number is octal instead of decimal for unit numbers greater than 7.

/U If the boot exists in the base ROM and also on the UBA, override the base ROM boot and use the UBA boot or M9312 module.

When using a switch, type the device name and unit number followed by / (slash) and the switches. When there is more than one switch, use only one slash.

If the BOOT command is entered without an argument, the ROM code prompts for additional information with the following message.

```
Enter device name and unit number then press the RETURN key:
```

At this point, if **?** (question mark) is typed, the ROM code lists the boot programs available, retypes the "Enter device name ...." message, and waits for a selection.

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key: B DL2 <CR>

Trying DL2

Starting system from DL2

RT-11FB (S) V05.01

.SET TT QUIE

.R DATIME
Date? [dd-mmm-yy]?
```

Figure 2-21 DL2 BOOT Example

2.7.3 LIST Command

Prints out a list of all available boot programs found in the CPU ROM, the CPU EEPROM, or any M9312-type ROMs located on the UBA or an M9312 module if present (Figure 2-22). Dialog mode is restarted at the completion of the LIST command.

The mnemonic for each ROM found on either the UBA or the M9312 will be checked against a list of mnemonics in the ROM code. If the mnemonic matches an item in this list, the ROM code will print out a description of that device. If no match is found, the description will be left blank for that mnemonic.

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key: L <CR>

Device Unit
name   numbers Source   Device type

 DU    0-255   CPU ROM  RD51, RD52, RX50, RC25, RA80, RA81, RA60
 DL    0-3     CPU ROM  RL01, RL02
 DX    0-1     CPU ROM  RX01
 DY    0-1     CPU ROM  RX02
 DD    0-1     CPU ROM  TU58
 DK    0-7     CPU ROM  RK05
 MU    0-255   CPU ROM  TK50, TU81

Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key:
```

Figure 2-22 LIST Command Display

2.7.4 SETUP Command

Setup mode is entered by typing the SETUP command (**S** and the **Return** key) in dialog mode. This mode allows the user to list or change parameters in the EEPROM, and also change bootstrap programs stored in the EEPROM.

When setup mode is first entered it prints out a list of its 15 commands and provides a short description of each (Figure 2-23).

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key: S <CR>

KDJ11-B Setup mode      KDJ11-B ROM V7.0

Command    Description

   1       Exit

   2       List/change parameters in the Setup table
   3       List/change boot translations in the Setup table
   4       List/change the Automatic boot selections in the table
   5       Reserved
   6       List/change the switch boot selections in the table
   7       List boot programs

   8       Initialize the Setup table

   9       Save the Setup table into the EEPROM
   10      Load EEPROM data into the Setup table

   11      Delete an EEPROM boot
   12      Load an EEPROM boot into memory
   13      Edit/create an EEPROM boot
   14      Save boot into the EEPROM
   15      Enter ROM ODT

Type a command then press the RETURN key:
```

Figure 2-23 SETUP Command Descriptions

Setup mode command notes:

1. The version number of the ROM code is printed out at the beginning of the setup mode message.

2. To execute a command, type the command number followed by the **Return** key.

3. Enter **<CTRL/C>** to return to dialog mode, or **<CTRL/Z>** to return to the beginning of setup mode.

4. Never terminate a parameter change with **<CTRL/C>** or **<CTRL/Z>**. If this is done the change is ignored and lost.

5. Always use the terminating character Return key after any change and then **<CTRL/C>** or **<CTRL/Z>**.

When setup mode is restarted by typing **<CTRL/Z>**, or at the completion of commands 2 thru 15, the ROM code will print out a short command message instead of the full list of commands (Figure 2-24). Enter a new command, or press the **Return** key to list the full command menu.

```
KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-24 Short Command Message

2.7.4.1 SETUP Command 1 – Exit command for setup mode. Returns the user to dialog mode. Dialog mode is also entered if **<CTRL/C>** is typed.

2.7.4.2 SETUP Command 2 – Causes the ROM code to print out the current status of all parameters, repeats the first parameter, and waits for user input (Figure 2-25). Type carriage returns to position the program at the desired parameter to be changed, or go directly to the parameter by typing the parameter letter.

NOTE
After changing any parameters in the setup table, command 9 (save) should be executed.

To change a parameter, type in the new value and press the **Return** key. Typing **<CR>**, **<LF>** or **.** (period) will cause the ROM code to proceed to the next parameter. Typing ^ or - will cause the ROM code to proceed to the previous parameter.

Figure 2-25 shows an example of command 2 being executed, and the value of parameters if command 8, (initialize setup table) had been executed.

```
 KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 2 <CR>

List/change parameters in the Setup table

A - ANSI Video terminal (1)              0=No,   1=Yes  = 1
B - Power up  0=Dialog, (1)=Automatic, 2=ODT, 3=24  = 1
C - Restart   0=Dialog, (1)=Automatic, 2=ODT, 3=24  = 1
D - Ignore battery                       0=No,   1=Yes  = 0
E - PMG 0-(7) 1=.4us, 2=.8, 3=1.6, 4=3.2,...7=25.6  = 7
F - Disable clock CSR                    0=No,   1=Yes  = 0
G - Force clock interrupts               0=No,   1=Yes  = 0
H - Clock  0=Power supply, 1=50Hz, 2=60Hz, 3=800Hz  = 0
I - Enable ECC test (1)                  0=No,   1=Yes  = 1
J - Disable long memory test             0=No,   1=Yes  = 0
K - Disable ROM 0=No, 1=Dis 165, 2=Dis 173, 3=Both  = 0
L - Enable trap on Halt                  0=No,   1=Yes  = 0
M - Allow alternate boot block           0=No,   1=Yes  = 0
N - Disable Setup mode                   0=No,   1=Yes  = 0
O - Disable all testing                  0=No,   1=Yes  = 0
P - Enable UNIBUS memory test (1)        0=No,   1=Yes  = 1
Q - Disable UBA ROM                      0=No,   1=Yes  = 0
R - Enable UBA cache (1)                 0=No,   1=Yes  = 1
S - Enable 18 bit mode                   0=No,   1=Yes  = 0
List/change parameters in the Setup table
Type <CTRL/Z> to exit or press the RETURN key for No change

ANSI Video terminal (1)          0=No,   1=Yes  = 0      New =
```

Figure 2-25 SETUP Command 2 Example

NOTE

If for any reason the N parameter (disable setup mode) is set to 1 (yes), the mode is disabled and cannot be entered.

If it is necessary to enter setup mode, set the FORCED DIALOGUE switch to ON, enter 2 <CR>, and reset parameter N to 0 (no).

If 124 KW of UNIBUS memory is present, the last two parameters will not be present (enable UBA cache and enable 18-bit mode). When this condition occurs, UBA cache is always disabled and 18-bit mode is unconditionally forced.

2.7.4.3 SETUP Command 3 – Prints out the contents of the translation table and allows changes to the table content (Figure 2-26). The translation table is used to allow devices to be booted using nonstandard CSR addresses.

The ROM code tries to find a match in the translation table for the device name and unit number. If no match is found the boot program uses the default CSR address for the device. If a match is found the translation table defines the CSR address used.

```
 KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 3 <CR>

List/change boot translations in the Setup table

TT1     blank
TT2     blank
TT3     blank
TT4     blank
TT5     blank
TT6     blank
TT7     blank
TT8     blank
TT9     blank

Type <CTRL/Z> to exit or press the RETURN key for No change

TT1     blank
Device name     =
```

Figure 2-26 SETUP Command 3 Example

The ROM code prompts for a new device name. If no translation table changes are desired, type **<CTRL/Z>** to return to the setup mode prompt. Skip over any entry by pressing the **Return** key. To enter a new device or change an entry, type in the new device name, unit number, and CSR address.

2.7.4.4 SETUP Command 4 – Allows selection of the devices to be tried in the automatic boot sequence (Figure 2-27). The user creates a small list that defines the devices and the order in which they are to be tried.

The example of Figure 2-27 shows that the user added the boot for the RX02 unit 1 (DY) by replacing the exit name (E) with DY and typing in the unit number. The exit function is moved to the next entry.

```
KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 4 <CR>

List/change the Automatic boot selections in the Setup table

A = Disk MSCP automatic boot
B = External ROM boot
E = Exit automatic boot
L = Loop continously

Boot 1 = A
Boot 2 = DL0
Boot 3 = MS0
Boot 4 = MU0
Boot 5 = E
Boot 6 = blank

Type <CTRL/Z> to exit or press the RETURN key for No change

Boot 1 = A
Device name      = <CR>

Boot 2 = DL0
Device name      = <CR>

Boot 3 = MS0
Device name      = <CR>

Boot 4 = MU0
Device name      = <CR>

Boot 5 = E
Device name      = DY <CR>
Unit number      = 1 <CR>

Boot 6 = blank
Device name      = E <CR>
Unit number      = 0 <CR>

KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-27 SETUP Command 4 Example

2.7.4.5 SETUP Command 5 – This command is reserved and is not used. If this command is entered, setup mode will be restarted and no changes are made.

2.7.4.6 SETUP Command 6 – Allows the user to define the value of three of the eight switches at the edge of the CPU module to boot specific devices (Figure 2-28). The command defines six of the eight possible combinations of switches 2–4. The other two combinations have a fixed definition that cannot be changed.

Figure 2-28 shows an example of command 6 with three of the six possible positions defined to select DU0, DU1, DU2, and the remaining three defined to select DL0.

```
KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 6 <CR>

List/change the switch boot selections in the Setup table

Switches 2,3,4  on   on   off   = DU0
Switches 2,3,4  on   off  on    = DU1
Switches 2,3,4  on   off  off   = DU2
Switches 2,3,4  off  on   on    = DL0
Switches 2,3,4  off  on   off   = DL0
Switches 2,3,4  off  off  on    = DL0

Type <CTRL/Z> to exit or press the RETURN key for No change

Switches 2,3,4  on   on   off   = DU0
Device name     =
```

Figure 2-28 SETUP Command 6 Example

2.7.4.7 SETUP Command 7 – Performs the same function as the LIST command in dialog mode, and is duplicated in setup mode for user convenience. Setup mode is restarted at the completion of this command.

2.7.4.8 SETUP Command 8 – Initializes the current contents of the setup table in memory to the default values (Figure 2-29). The command does not affect the contents of the EEPROM itself. Command 9 must be executed in order to save the setup table into the EEPROM. Command 8 only affects parameters associated with commands 2 through 6.

The following items list the value of the parameters after command 8 is executed:

- All parameters listed under command 2 of are set to 0 with the exception of A, B, C, I, P, and R which are set to 1 (Figure 2-25).
- All entries in the translation table under command 3 are cleared and will list as blank.
- The automatic boot selection list under command 4 will be set to A, DL0, MS0, MU0, E, blank.

Enter the command by typing **8** and the **Return** key. After the ROM code prompt, type **1** and the **Return** key. Command 9 (save) should be executed after command 8 to copy the defaults into the EEPROM.

```
KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 8 <CR>

Initialize the Setup table

Are you sure ?  0=No,   1=Yes
Type a command then press the RETURN key: 1 <CR>

KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-29 SETUP Command 8 Example

2.7.4.9 SETUP Command 9 – Copies the current contents of the setup table in memory into the EEPROM (Figure 2-30). The command should be executed after any changes are made.

If command 9 is entered and no changes have been made to the setup table, the ROM code will output a message stating that no changes were made and then restart setup mode. If changes are to be made, the ROM code will prompt to ensure changes are desired.

```
KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 9 <CR>

Save the Setup table into the EEPROM

Are you sure ?  0=No,   1=Yes
Type a command then press the RETURN key: 1 <CR>

Writing the EEPROM

KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-30 SETUP Command 9 Example

2.7.4.10 SETUP Command 10 – Restores the setup table in memory with the values actually stored in the EEPROM, and allows the user to restore the setup table after making some temporary changes (Figure 2-31). It is also used to load the actual data from the EEPROM into the setup table if an error occurred during the EEPROM checksum tests.

When an error occurs during the EEPROM checksum tests, the ROM code assumes the data is bad and loads a set of default values into the setup table and uses them. In this case, the user could load the actual data and then verify that the data is good before trying to save it in the EEPROM.

```
 KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 10 <CR>

Load EEPROM data into the Setup table

Are you sure ?  0=No,   1=Yes
Type a command then press the RETURN key: 1 <CR>

KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-31 SETUP Command 10 Example

2.7.4.11 SETUP Command 11 – Allows the user to delete an EEPROM boot (Figure 2-32). The ROM code will prompt for the device name of the EEPROM boot to be deleted. After the device name is entered, the ROM code searches for the first boot program in the EEPROM with that device name and deletes it.

If there are any boot programs following the deleted program, the ROM code automatically moves these programs up to use the space made available by the deleted program.

```
 KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 11 <CR>

Delete an EEPROM boot

Type <CTRL/Z> to exit or press the RETURN key for No change

Device name      = CC <CR>

Are you sure ?  0=No,   1=Yes
Type a command then press the RETURN key: 1 <CR>

KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-32 SETUP Command 11 Example

2.7.4.12 SETUP Command 12 – Copies an EEPROM boot program into memory (Figure 2-33). The ROM code prompts for the device name of the EEPROM boot program to be loaded in memory. The program can then be examined and/or edited using SETUP command 13.

```
KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 12 <CR>

Load an EEPROM boot into memory

Type <CTRL/Z> to exit or press the RETURN key for No change

Device name      = CC <CR>

Are you sure ?  0=No,   1=Yes
Type a command then press the RETURN key: 1 <CR>

KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-33 SETUP Command 12 Example

2.7.4.13 SETUP Command 13 – Used to create a new EEPROM boot program, or to edit a program previously loaded with command 12. Command 13 allows changes to the device name, device description, allowable unit number range, beginning and ending addresses of the program in memory, and the starting address of the program (Figure 2-34).

When changes are complete the ROM code enters ROM ODT. When the command is first entered it will list the available space in the EEPROM for bootstrap programs

```
KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 13 <CR>

Edit/create an EEPROM boot

Type <CTRL/Z> to exit or press the RETURN key for No change

1410 Bytes free in the EEPROM

Device name              = AA            New = EA <CR>

Beginning  address       = 000600        New = 10000 <CR>

Last byte address        = 000615        New = 10177 <CR>

Start address            = 000600        New = 10000 <CR>

Highest Unit number      = 3             New = 255 <CR>

Device Description       = EA BOOT       New = RM02,RM03 <CR>

Enter ROM ODT

xxxxxx/ = open word location xxxxxx if address even, byte if odd
RETURN  = close location
. or LF = close location and open next
-       = close location and open previous

ROM ODT> 010000/000000 012705 <CR>
ROM ODT> 010002/000000 101 <CR>
ROM ODT> 010004/000000 12706 <CR>
ROM ODT> 010006/000000 1000 <CR>
etc.     Type <CTRL/Z> exit back to the setup mode menu.
```

Figure 2-34 SETUP Command 13 Example

2.7.4.14 SETUP Command 14 – Allows the user to save the existing boot program located in memory into the EEPROM. This is the only command that actually writes a boot into the EEPROM (Figures 2-35 and 2-36). The other commands only change a copy of the boot program that resides in memory.

When saving a boot program in memory, the device name of the program must not match the name of an existing program in the EEPROM. If the program name already exists, delete that program first or change the name of the program to be saved. If two or more programs were written into the EEPROM with the same name, only the first will be used.

```
 KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 14 <CR>

Save boot into the EEPROM

Type <CTRL/Z> to exit or press the RETURN key for No change

Are you sure ?  0=No,   1=Yes
Type a command then press the RETURN key: 1 <CR>

Writing the EEPROM - Please wait

KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-35 SETUP Command 14, Example 1

```
KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 14 <CR>

Save boot into the EEPROM

Boot is already in the EEPROM

No changes made

KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-36 SETUP Command 14, Example 2

2.7.4.15 SETUP Command 15 – Calls ROM ODT. The ROM code will open up the address defined by the beginning address of the program (Figure 2-37).

NOTE

ROM ODT is not the same as J11 micro ODT. Its only purpose is to allow the user to create or edit a small bootstrap program to be stored in the EEPROM.

In ROM ODT, the only addresses that can be examined are memory addresses from 0 – 28 KW (0 – 00157776). Table 2-10 lists the ROM ODT commands.

Table 2-10 ROM ODT Commands

Command	Symbol	Use
Slash	/	Prints contents of specified location. If no address is defined, then print contents of the last location that was opened. If location opened is an odd number, print out only the contents of the byte. If location is even, then mode is word; if location is odd, then mode is byte. Leading zeroes are assumed. Only bits 15 through 0 of the address are used.
Return	<CR>	Closes an open location.
Line Feed	<LF>	Closes an open location and opens the next location. If word, increment address by 2; if byte, increment address by 1.
Period	.	Alternate character for line feed. This command is useful when the terminal is a VT2xx series terminal. It is also convenient to use with the keypad.
Up Arrow	^	Closes an open location and opens the previous location. If in word mode, decrement by 2; if byte, decrement by 1.
Minus	–	Alternate character for up arrow. This command is useful when the terminal is a VT2xx series terminal. It is also convenient to use with the keypad.
Delete	DELETE	Deletes the previous character typed.
<CTRL/Z>	^Z	Exit ROM ODT and return to setup mode.

The following paragraphs present examples of ROM ODT use.

Example 1:

Location 200 is opened. It is then closed with no changes and location 202 is opened, which is then closed after changing its contents.

```
ROM ODT > 200/
ROM ODT > 000200/100000 <LF>
ROM ODT > 000202/003333 44 <CR>
ROM ODT >
```

Example 2:

Byte location 1001 is opened. It is then closed and locations 1002 and 1003 are opened. Data in location 1003 is changed and the location is closed.

```
ROM ODT > 1001/
ROM ODT > 001001/101 <LF>
ROM ODT > 001002/104 <LF>
ROM ODT > 001003/113 141 <CR>
ROM ODT >
```

Example 3:

The user attempts to open location 170 000 which is in the I/O page and not allowed.

```
ROM ODT > 77770000/
ROM ODT >
```

Example 4:

Location 150 000 is opened and closed. It is then reopened by typing / (slash) only.

```
ROM ODT > 150000/
ROM ODT > 150000/032737 <CR>
ROM ODT > /
ROM ODT > 150000/032737
```

Figure 2-37 presents an example of command 15.

```
KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key: 15 <CR>

Enter ROM ODT

Type <CTRL/Z> to exit or press the RETURN key for No change

xxxxxx/ = open word location xxxxxx if address even, byte if odd
RETURN  = close location
. or LF = close location and open next
-       = close location and open previous

ROM ODT> 010000/000000 012705 <CR>
ROM ODT> 010002/000000 101 <CR>
ROM ODT> 010004/000000 12706 <CR>
ROM ODT> <CTRL/Z>

KDJ11-B Setup mode
Press the RETURN key for Help
Type a command then press the RETURN key:
```

Figure 2-37 SETUP Command 15 Example

2.7.5 MAP Command

Identifies all memory in the system and then maps all locations in the I/O page (Figure 2-38). Dialog mode is restarted at completion of the MAP command.

NOTE

If two memories share some common addresses or have CSRs with the same address, the command will not work properly.

During mapping, if two or more memories are present and they are not contiguous, the ROM code will separate their descriptions with a blank line.

The ROM code waits for the user to press the **Return** key anytime the data on the video screen might overflow.

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key: M <CR>

Memory Map
Starting   Ending       Size in    CSR          CSR      Bus
Address    address      K Bytes    address      type     type

00000000 - 03777776     1024       17772100     Parity   PMI

Press the RETURN key when ready to continue <CR>

I/O page Map
Starting   Ending
Address    address

17765000 - 17765776     CPU ROM or EEPROM
17770200 - 17770376     Unibus Map
17772100                Memory CSR
17772150 - 17772152
17772200 - 17772276     Supervisor I and D PDR/PAR's
17772300 - 17772376     Kernel I and D PDR/PAR's
17772516                MMR3
17773000 - 17773776     CPU ROM or UBA ROM
17774400 - 17774406
17777520 - 17777524     BCSR, PCR, BCR/BDR
17777546                Clock CSR
17777560 - 17777566     Console SLU
17777572 - 17777576     MMR0,1,2
17777600 - 17777676     User I and D PDR/PAR's
17777730 - 17777734     DCSR, DDR, KMCR
17777744 - 17777752     MSER, CCR, MREG, Hit/Miss
17777766                CPU Error
17777772                PIRQ
17777776                PSW

Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key:
```

Figure 2-38 MAP Command Display

2.7.6 TEST Command

The TEST command causes the ROM code to run most of the power up tests in a continous loop. The code starts at test 70 and restarts the loop after test 30. If an error occurs, the general error routine is entered.

Exit the test loop by typing **<CTRL/C>** at the console. When the test loop is exited, the ROM code will print out the total number of loops and the total number of errors (if any).

A test number may also be entered after the TEST command. If applicable, the ROM code will loop on that specific test until an error occurs or **<CTRL/C>** is typed. If the test number is not a loopable test, the general test loop will be entered and all loopable tests will be run.

NOTE

<CTRL/C> is not echoed by the ROM code on the console terminal.

Figure 2-39 shows an example of entering the test command by typing **T** and the **Return** key which runs all loopable tests. The testing sequence is aborted after four passes by typing **<CTRL/C>**.

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key: T <CR>

Continuous self test - Type <CTRL/C> to exit <CTRL/C>

Total Passes = 4
Total Errors = 0

Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key:
```

Figure 2-39 TEST Command Example

Figure 2-40 shows an example of looping on only test 60. The test loop is aborted by typing **<CTRL/C>** after 202 passes.

```
Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key: T 60 <CR>

Looping on test 60 - Type <CTRL/C> to exit <CTRL/C>

Total Passes = 202
Total Errors = 0

Commands are Help, Boot, List, Setup, Map and Test.
Type a command then press the RETURN key:
```

Figure 2-40 Loop-on-Test Example

CHAPTER 3
REMOVAL AND REPLACEMENT PROCEDURES

3.1 FIELD REPLACEABLE UNITS

Table 3-1 lists the field replaceable units (FRU) for the P-series systems. Table 3-2 lists the FRUs for the A-series.

Table 3-1 P-Series FRU Descriptions

Part Number	Description
M7677	Monitor distribution module (MDM)
M8191	KTJ11-B, UBA module
M8190	KDJ11-BC, CPU module
M7458-A	MSV11-RA, 1Mbyte parity memory
M7556	Minimum load module
M9302	Terminator module
70-20650-01	CPU backplane
H7202-KA	Power supply
H7202-KB	Power supply
54-16508-01	Console SLU board
H7211-B *	+15V, −15V regulator module
H7213-D *	+12V, +5V regulator module
H7200-C *	+5V regulator module
70-21888-01	Front panel assembly
12-22001-01	Blower
12-22271-02	Fan
877-D	Power controller 120V
877-F	Power controller 240V
70-21116-01	Circuit-breaker assembly

* Specifies minimum etch revision.

Table 3-2 A-Series FRU Descriptions

Part Number	Description
M7677-YA *	Monitor distribution module
M8191	KTJ11-B, UBA module
M8190	KDJ11-BF, CPU - FPA module
M8637-BA	MSV11-JB, 1 Mbyte ECC memory
M8637-CA	MSV11-JC, 2 Mbyte ECC memory
M7556	Minimum load module
M9302	Terminator module
70-20650-01	CPU backplane
H7202-KA	Power supply
H7202-KB	Power supply
54-16508-01	Console SLU board
H7211-B **	+15V, −15V regulator module
H7213-D **	+12V, +5V regulator module
H7200-C **	+5V regulator module
70-21888-01	Front panel assembly
12-22001-01	Blower (cabinet)
12-22271-02	Fan (box)
877-D	Power controller 120V
877-F	Power controller 240V
70-21116-01	Circuit-breaker assembly
Options:	
H7231-E	Battery-backup unit
DD11-CK	4-slot backplane
DD11-DK	9-slot backplane

* M7677-YA must be installed if the system contains the H7231-E BBU option.
** Specifies minimum etch revision.

3.2 GENERAL MODULE REMOVAL/REPLACEMENT

To remove any module listed in Tables 3-1 and 3-2 (except the CPU module) use the following procedure.

CAUTION

1. **Modules are static sensitive.**
2. **Always wear a properly connected ground strap when handling modules.**
3. **Modules must be placed on a static mat anytime they are removed from a backplane or their shipping static bags.**

1. Open the cabinet front and rear doors using the hex key, or slide the box out of the rack.
2. Turn either:
   a. The cabinet power supply and power controller circuit breakers to OFF, or
   b. The box circuit breaker to OFF.
3. Remove the ac power cord from the outlet.
4. Ensure that the ground strap is properly connected.
5. Remove all cables from the module and label each one.
6. Pull the module handles out and slide the module from the backplane.
7. Place the module on the static mat.

This completes the removal of a module. To reinstall a module, reverse the procedure.

3.3 CPU MODULE REMOVAL/REPLACEMENT

Replacing the CPU module is a special case. The replacement module setup features must be confirmed and, if necessary, revised to the original CPU parameters and selections.

During the initial system installation, the user should have recorded the setup feature selections on the worksheet supplied in the *Installation Guide* or Appendix B in this guide. Retrieve this form. Compare the selections of the original CPU module (as specified on the worksheet) with the factory-set defaults of the replacement module.

Confirm and/or revise the setup features using the following procedure.

NOTE

Dialog and setup mode commands are described in subsection 2.7.

1. Wear a properly connected ground strap. Remove the defective module from the backplane as specified in subsection 3.1.

2. Ensure that the replacement module jumper configurations and DIP switch settings are as specified in subsection 2.7.3.

3. Install the replacement CPU module as described in subsection 3.2.

4. Set the forced dialogue switch to ON.

5. Power-up the system, and ensure that it passes the startup diagnostics.

6. On successful cpmletion of the startup diagnostics, the system enters dialog mode (Figure 2-19).

7. Enter setup mode by typing **S** and the **Return** key on the console terminal (Figure 2-23).

8. If the customer chose the factory defaults, perform steps 8 and 9; otherwise, begin at step 10.

9. Type **8** and the **Return** key to initialize the setup table to the factory default values. Type **1** and the **Return** key at the ROM code prompt (Figure 2-29).

10. Type **9** and the **Return** key to copy the default values to the EEPROM. Type **1** and the **Return** key at the ROM code prompt (Figure 2-30).

11. Type **2** and the **Return** key to display the setup table parameters (Figure 2-25). Compare the replacement module parameters to the original selections; revise as required.

12. Type **3** and the **Return** key to display the translation table parameters (Figure 2-26). Compare the parameters to the original selections; revise as required.

13. Type **4** and the **Return** key to display the automatic boot selections (Figure 2-27). Compare the selections to the original; revise as required.

14. Type **6** and the **Return** key to display the CPU switch boot selections (Figure 2-29). Compare the selections to the original; revise as required.

15. Type **9** and the **Return** key to copy the revised parameters and selections into the EEPROM (Figure 2-30). Type **1** and the **Return** key at the ROM code prompt.

16. Type **1** and the **Return** key to exit setup mode and return to dialog mode.

This completes the CPU module replacement and setup procedure.

3.4 POWER SUPPLY REMOVAL/REPLACEMENT

Both the cabinet and box products have H7202-KA power supplies each containing three regulator boards. The regulator boards and power supplies are FRUs. Make sure that the regulator boards are not defective prior to replacing a power supply.

3.4.1 Cabinet Power Supply Removal/Replacement

To remove a power supply regulator board or the main power supply, use the following procedure.

1. Open the front and rear doors using the hex key.
2. Turn off the power supply and power controller circuit breakers.
3. Remove the ac power cord from the outlet.
4. Loosen the two captive screws holding the blower assembly.
5. Slide the blower assembly out about four inches, and disconnect the blower motor power cable.
6. Slide the blower assembly out and up to remove it from the cabinet assembly (Figure 3-1).

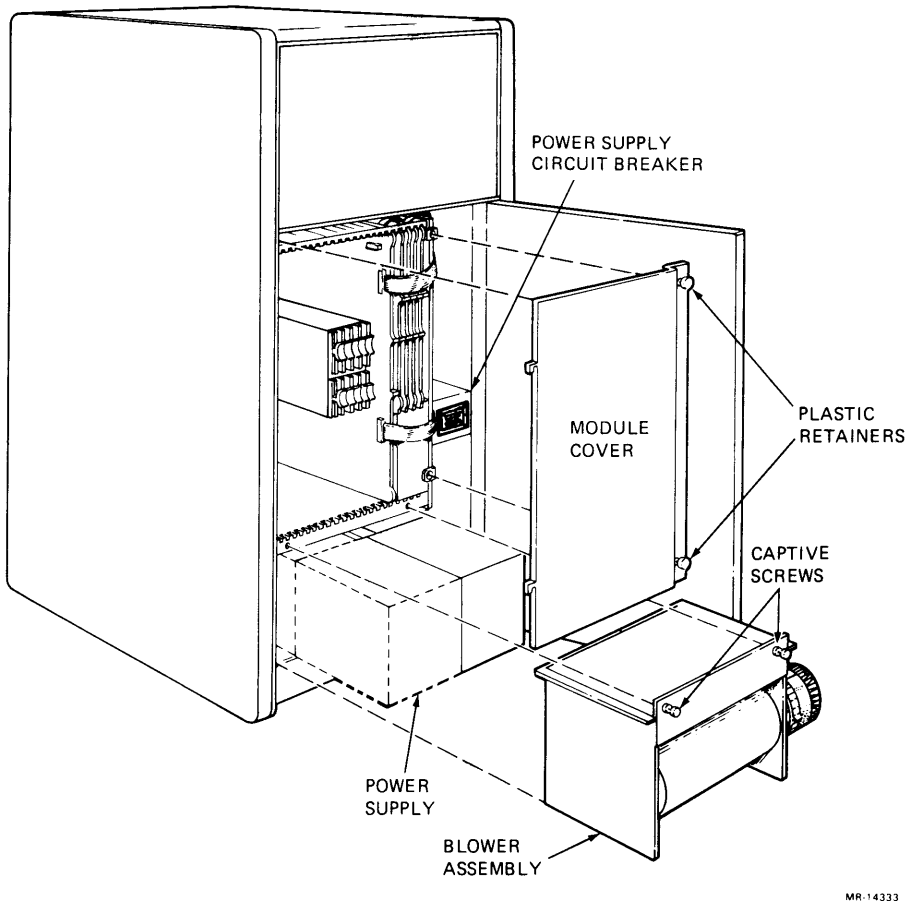

Figure 3-1 Blower Assembly Removal

7. Push in the power supply tray lock (located on the left edge of the tray slide). Slide the tray out by pulling on the tray handle until the second tray lock engages (Figure 3-2).

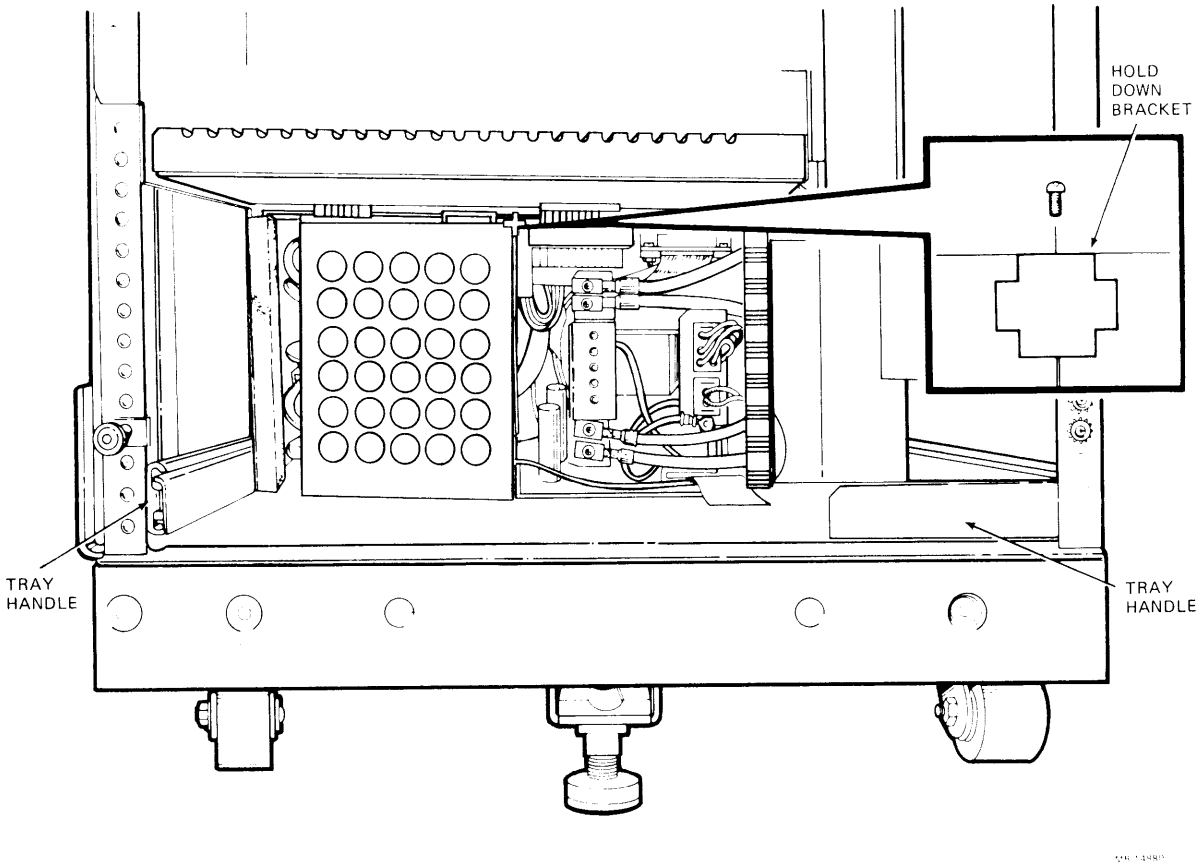

Figure 3-2 Cabinet Power Supply Removal

8. Loosen and remove the power supply hold-down bracket located near the top left edge of the power supply.

9. Using a Phillips-head screwdriver, remove the four 5 Vdc bus wires.

10. Remove the two ribbon cables and the ac input cable.

11. Using a 3/8-inch wrench, remove the ground lug.

12. Pull the power supply forward and remove it from the cabinet.

13. Loosen the three captive screws holding the top cover of the power supply and remove the cover (Figure 3-3).

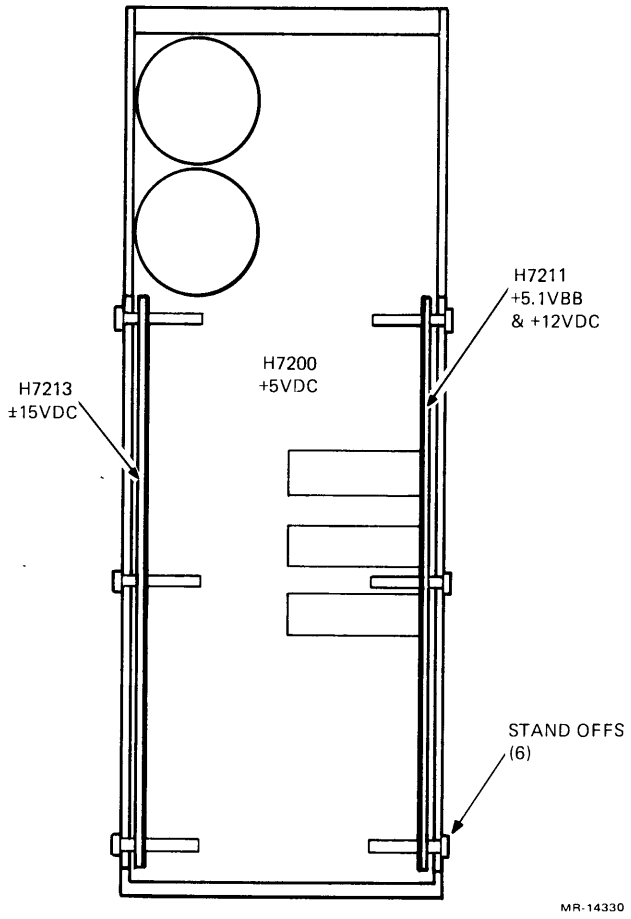

Figure 3-3 Power Supply Regulator Removal

14. To remove the memory/fan (H7213) or the communications option (H7211) regulators, gently lift them out by grasping each corner standoff and lift up.

15. To remove the H7200 regulator, turn the power supply over (open side down), and while supporting the regulator, loosen the six Phillips-head screws securing it to the chassis.

16. Remove the regulator from the chassis.

This completes the removal of the regulators boards and power supply. To reinstall, reverse the above procedure.

3.4.2 Box Power Supply Removal

To remove a power supply regulator or power supply, use the following procedure.

1. Turn off the circuit breaker.
2. Unplug the ac power cord from the outlet.
3. Remove the box top cover by removing the four captive screws and lifting the cover off.
4. Loosen the two Phillips-head screws on the power supply cover. Slide the cover backwards and lift to remove it (Figure 3-4).

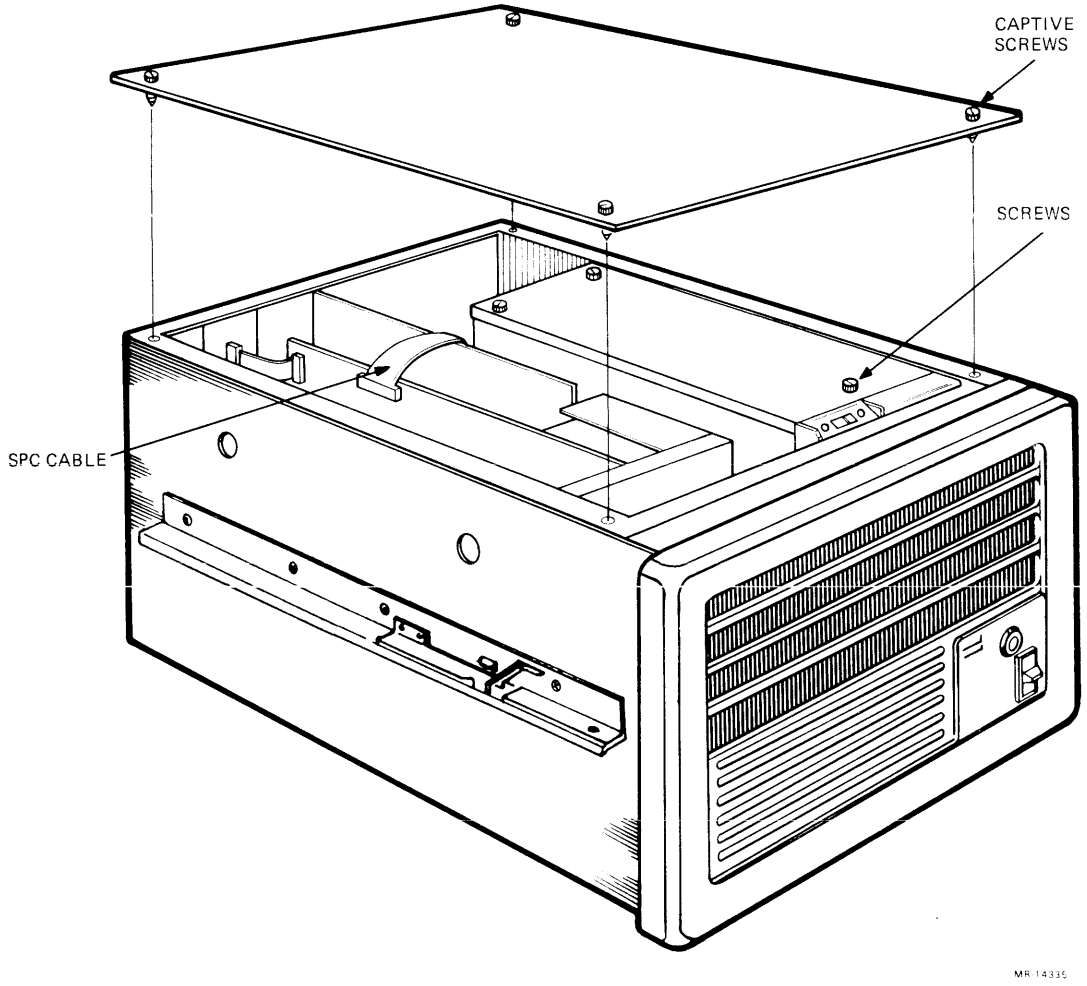

Figure 3-4 Power Supply Removal

5. To remove either the memory/fan (H7213) or the communications option (H7211) regulators, gently lift them out by grasping the two corner standoffs and lift up.

6. To remove the H7200 regulator, the power supply must be removed from the box. Loosen the four screws that secure the power supply to the chassis shelves. Lift the power supply out of the box (Figure 3-5).

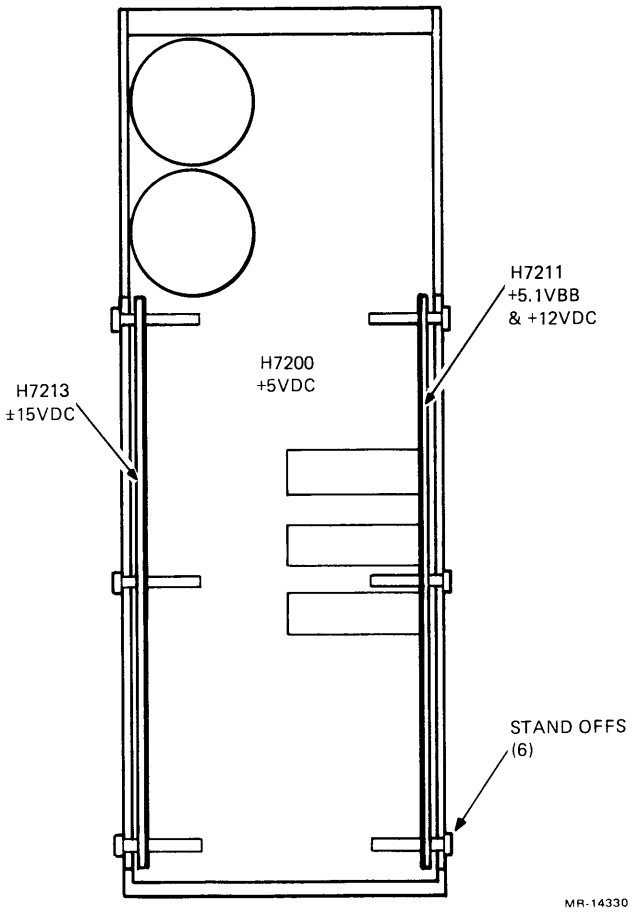

Figure 3-5 Power Supply Regulator Removal

7. After removal, turn the power supply over (open side down) and while supporting the regulator, loosen the six Phillips-head screws securing it to the chassis.

8. Remove the regulator from the chassis.

NOTE
If the power supply is replaced, set the 120/240 ac voltage select switch to match the site line voltage.

This completes the removal procedure for box power supply and regulators. To reinstall the regulators and power supply, reverse the above procedure.

3.5 CABINET BLOWER REMOVAL/REPLACEMENT

To remove the blower assembly use the following procedure.

1. Open the front and rear doors using the hex key.
2. Turn off the power supply and power controller circuit breakers.
3. Remove the ac power cord from the outlet.
4. Loosen the two captive screws holding the blower assembly. Slide the blower assembly out about four inches. Disconnect the blower motor power cable.
5. Slide the blower assembly out while lifting up, and remove it from the cabinet (Figure 3-6).

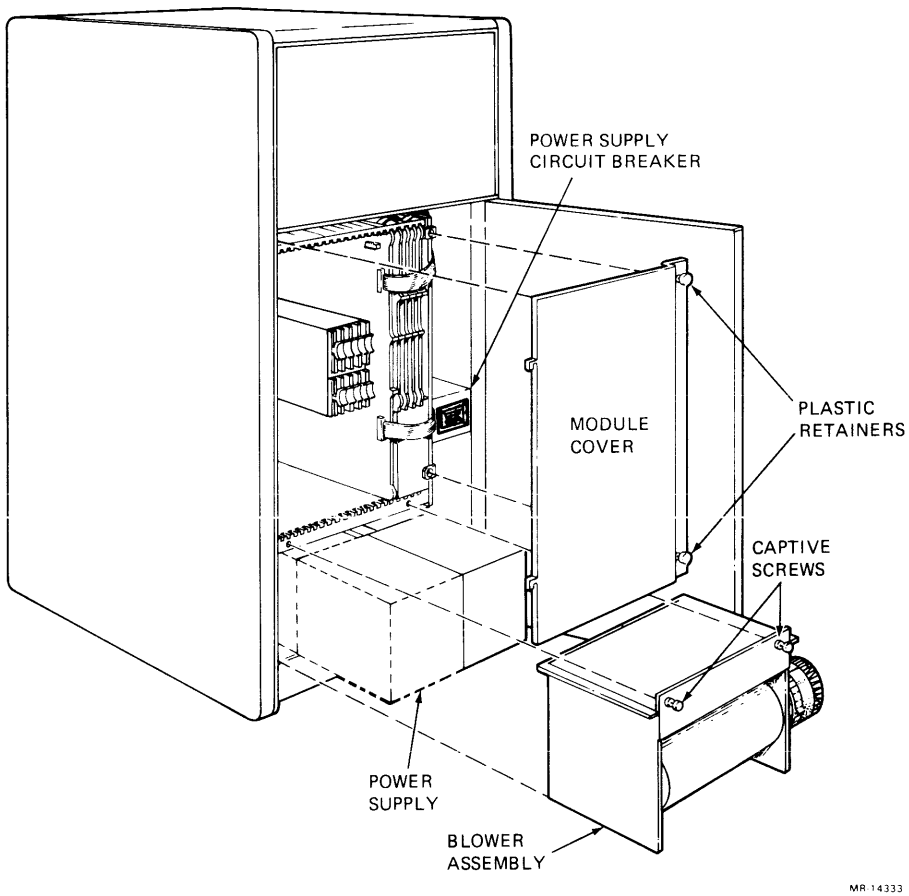

Figure 3-6 Blower Assembly Removal

This completes the removal procedure for the cabinet blower assembly. Reinstall the blower assembly in the reverse order.

3.6 BOX FAN REMOVAL/REPLACEMENT

There are three fans used in the box product. Two fans cool the module card cage and the third cools the power supply. To remove any one of the fans use the following procedure.

1. Turn off the circuit breaker.
2. Unplug the ac power cord from the outlet.
3. Remove the four screws from the rear of the box flange. Remove the bezel from the box.
4. Loosen the six captive screws from the metal grid in front of the fans. Lift off the metal grid.
5. Loosen the two Phillips-head screws securing the fan to its mounting position on the plenum (Figure 3-7).

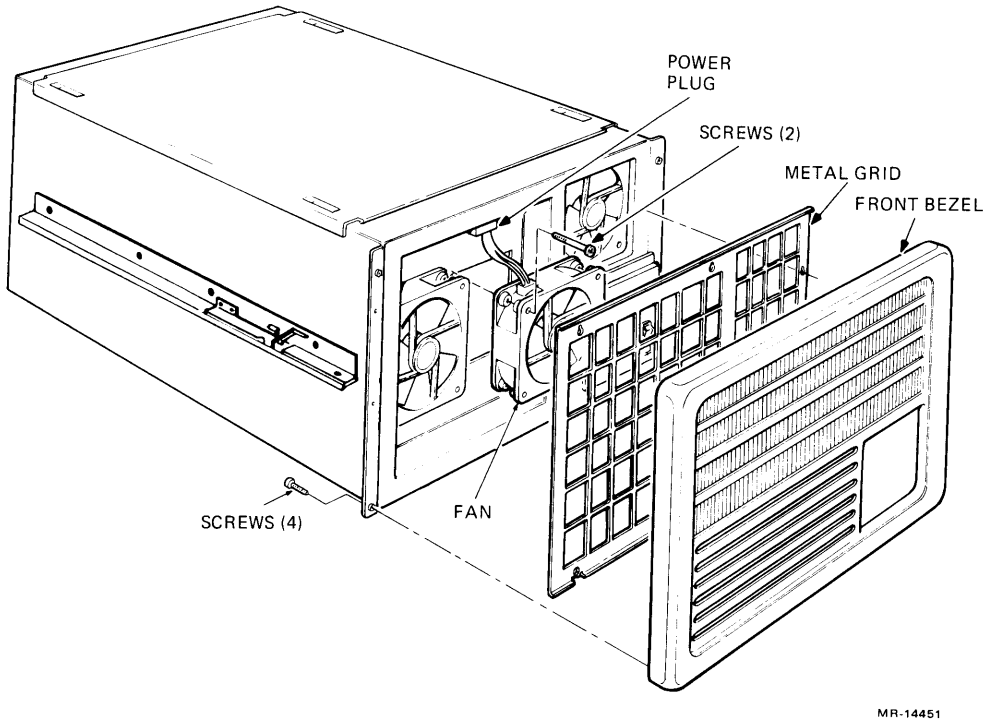

Figure 3-7 Box Fan Removal

6. Unplug the fan power cable and remove the fan.

CAUTION

When installing a fan, ensure that the airflow arrow points toward the plenum.

When installing a replacement fan, tighten the mounting screws snug. Do not overtighten.

This completes the fan removal procedure. To reinstall a new fan, reverse the above procedure.

3.7 FRONT PANEL REMOVAL/REPLACEMENT

The cabinet and box front panels are identical, but have different removal and replacement procedures.

3.7.1 Cabinet Front Panel Removal/Replacement

To remove the cabinet front panel use the following procedure.

1. Open the front and rear doors using the hex key.
2. Turn off the power supply and power controller circuit breakers.
3. Remove the ac power cord from the outlet.
4. Disconnect the cable from the front panel assembly (Figure 3-8).

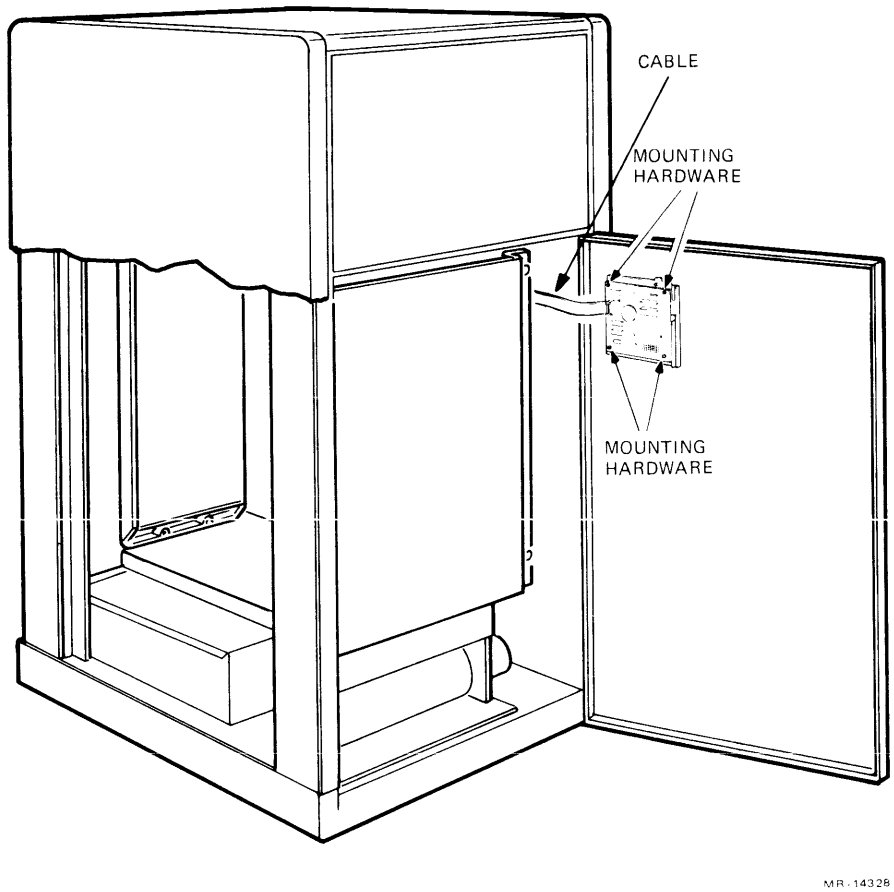

Figure 3-8 Cabinet Front Panel Removal

5. Remove the four 3/8-inch nuts holding the front panel to the door.
6. Remove the front panel from the standoffs.

This completes the removal of the cabinet front panel assembly. To reinstall the front panel, reverse the above procedure.

3.7.2 Box Front Panel Removal/Replacement

To remove the box front panel use the following procedures.

1. Turn off the power supply circuit breaker.
2. Unplug the ac power from the outlet.
3. Remove the front bezel by loosening and removing the four screws from the bezel rear side. Pull the bezel away from the box (Figure 3-9).

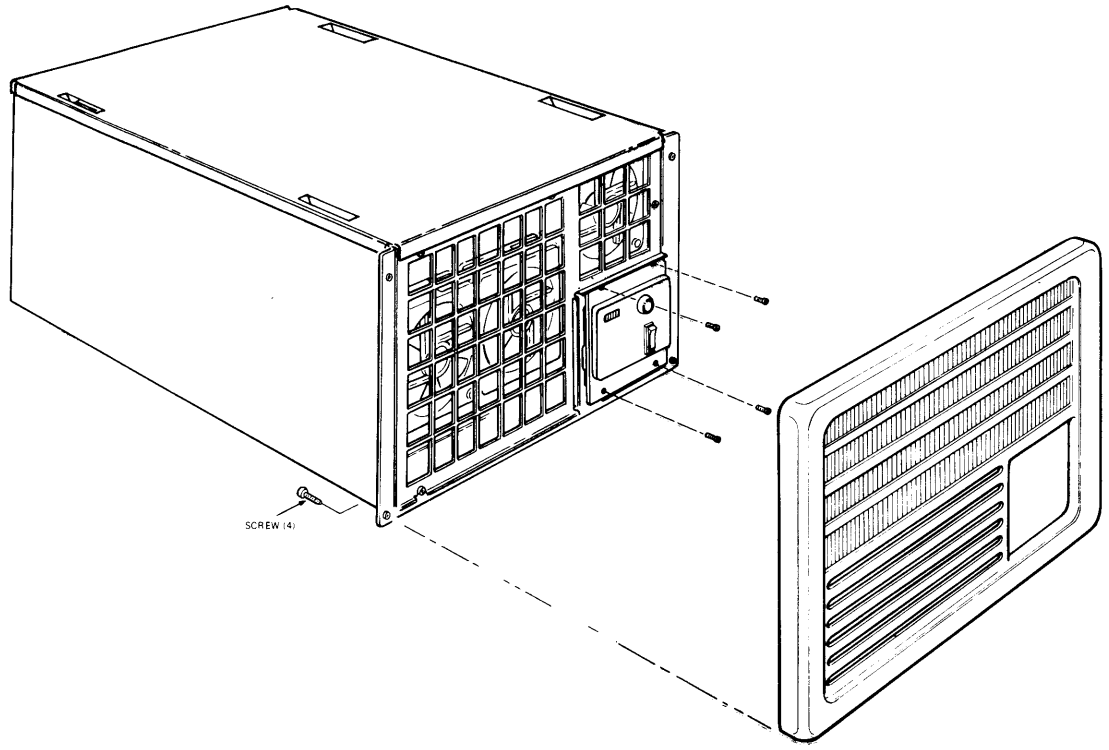

Figure 3-9 Front Panel Removal

4. Remove the cable that is plugged into the front panel assembly.
5. Loosen and remove the four Phillips-head screws securing the front panel to the chassis.
6. Remove the front panel assembly.

This completes the removal of the front panel. To reinstall the box front panel, reverse the above procedure.

3.8 CIRCUIT BREAKER REMOVAL/REPLACEMENT

Both products have circuit breakers for their power supplies. The box circuit breaker assembly is located externally on the right side. The cabinet circuit breaker is located internally, and has two breakers: the main power supply and the expansion power supply.

3.8.1 Cabinet Circuit Breaker Removal/Replacement

To remove the circuit breaker assembly use the following procedure.

1. Open the front and rear doors using the hex key.
2. Turn off the power supply and power controller circuit breakers.
3. Remove the ac power cord from the outlet.
4. Unplug the cords connected to the assembly (Figure 3-10).

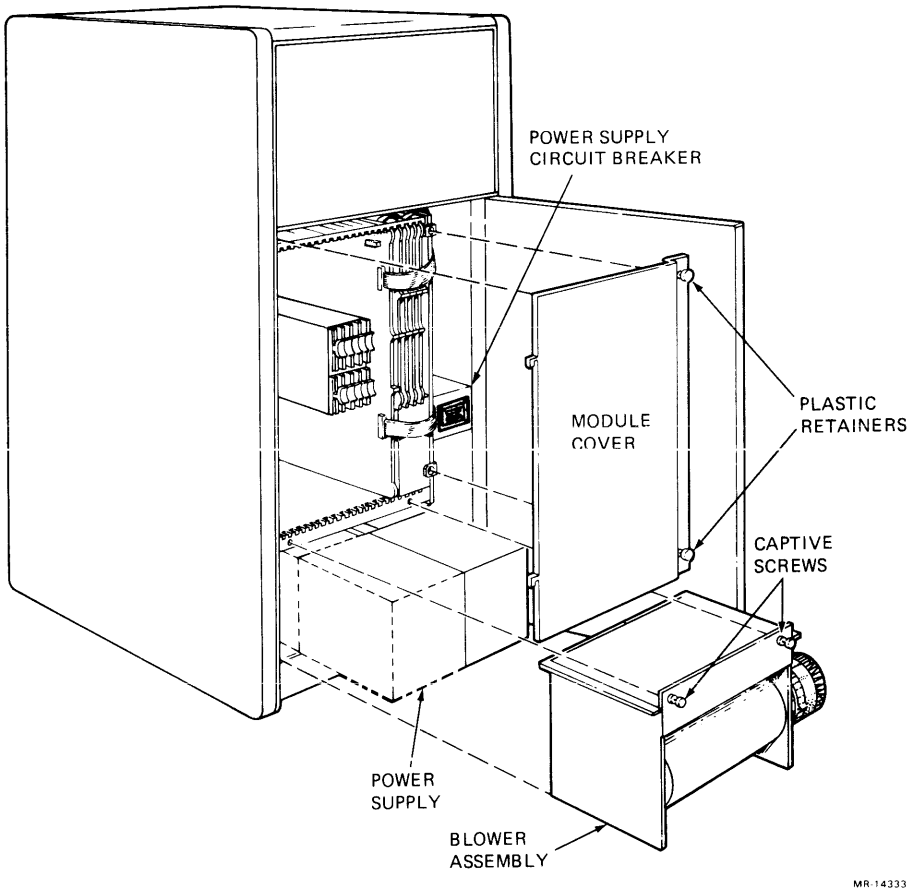

Figure 3-10 Cabinet Circuit Breaker Removal

5. Remove the blower power connector by pushing in on the connector release clips and pulling the connector loose.

6. Loosen the two screws securing the circuit breaker assembly to the cabinet support and remove the assembly.

This completes the removal of the circuit breaker assembly.

To reinstall the assembly, reverse the above procedures. Ensure that the power cable plugged into the unswitched power controller outlet is inserted into J1.

3.8.2 Box Circuit Breaker Removal/Replacement

To remove the circuit breaker assembly, use the following procedures.

1. Turn off the circuit breaker.

2. Unplug the ac power cord from the outlet.

3. Remove the rear four bulkhead sections marked A1 through A4. Each section has two flathead screws (Figure 3-11).

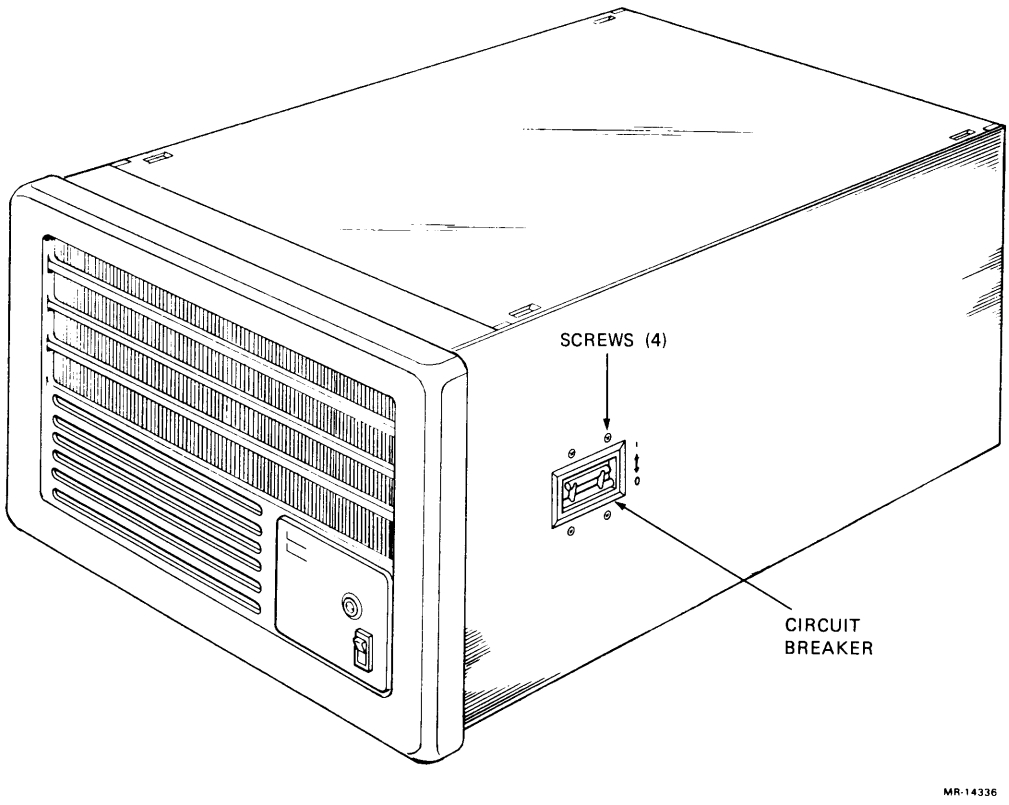

Figure 3-11 Box Circuit Breaker Removal

4. Remove the four screws securing the breaker assembly to the box.

5. Reach inside the box through the bulkhead access and release the three cable clips along the box wall.

6. Remove the circuit breaker through the rear bulkhead access.

7. Remove the four screws securing the wires on the back of the circuit breaker. Label each wire.

This completes the replacement procedure for the circuit breaker assembly. To reinstall the circuit breaker, reverse the procedure.

3.9 CABINET POWER CONTROLLER REMOVAL/REPLACEMENT

To remove the 877 power controller assembly, use the following procedure.

1. Open the front and rear doors using the hex key.

2. Turn off the power supply and power controller circuit breakers.

3. Remove the ac power cord from the outlet.

4. Lift the left side panel straight up from both sides. Be careful—the outside panel is heavy (Figure 3-12).

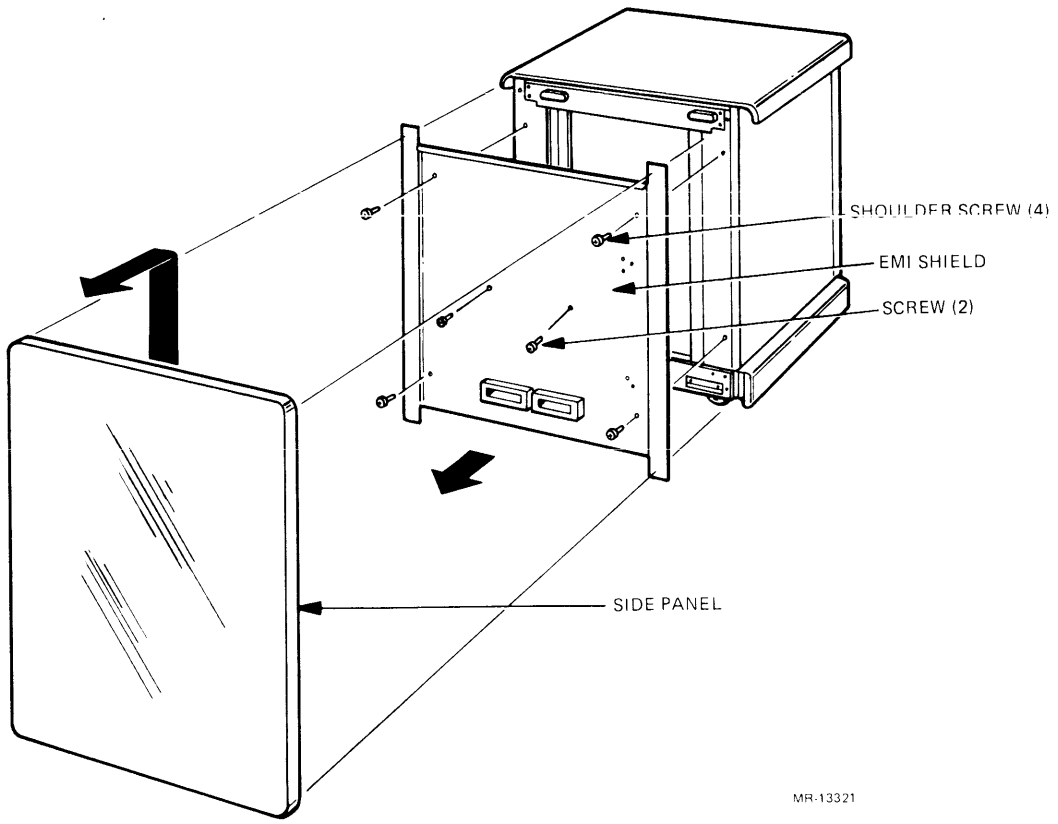

Figure 3-12 Cabinet Side Panel Removal

5. Remove the two Phillips and four shoulder screws securing the EMI shield to the cabinet side.

6. Label each power plug and its receptacle, and remove the plugs (Figure 3-13).

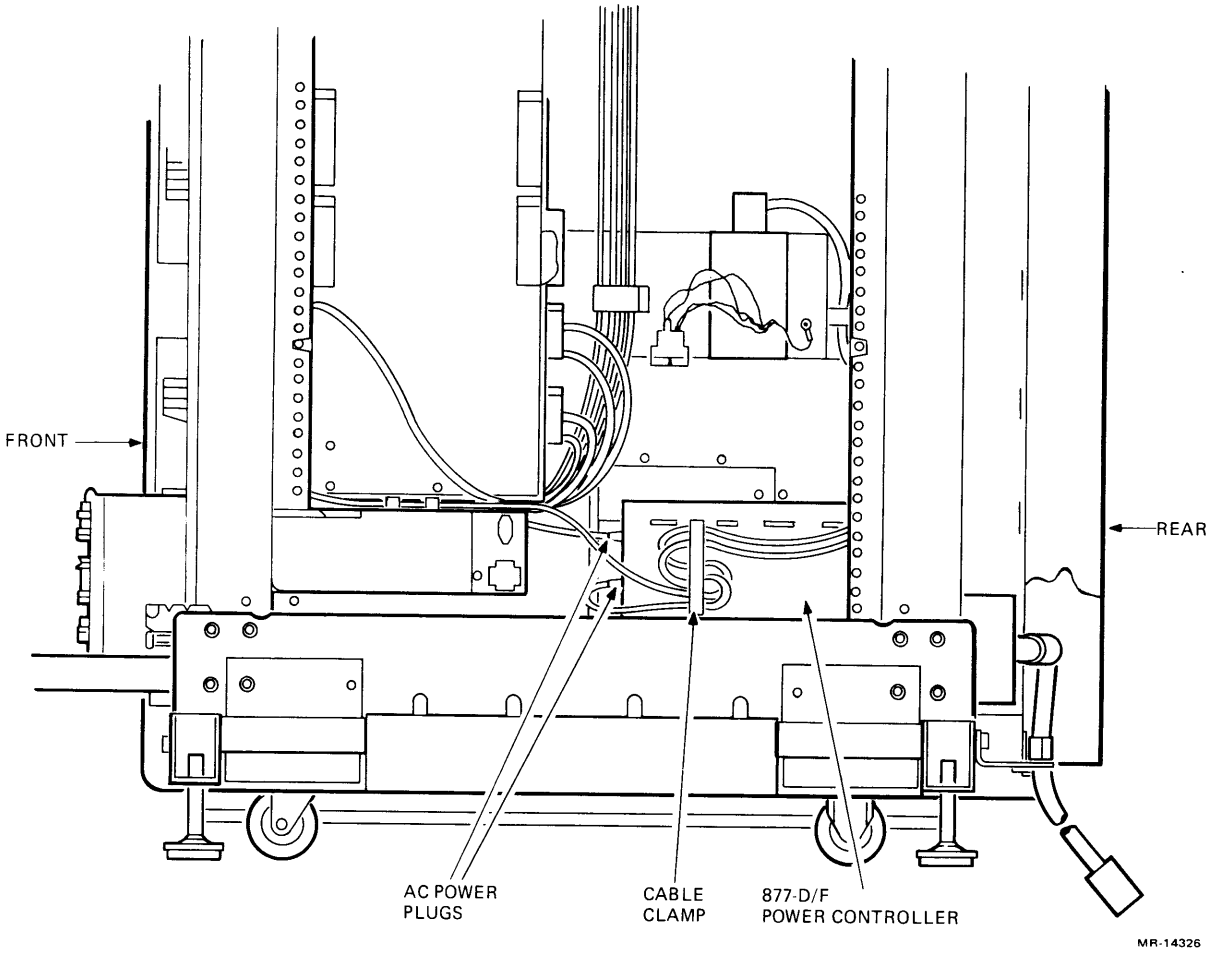

Figure 3-13 Power Controller Removal – Side View

7. Loosen the 10 Phillips-head screws securing the power controller to the cabinet bulkhead (Figure 3-14).

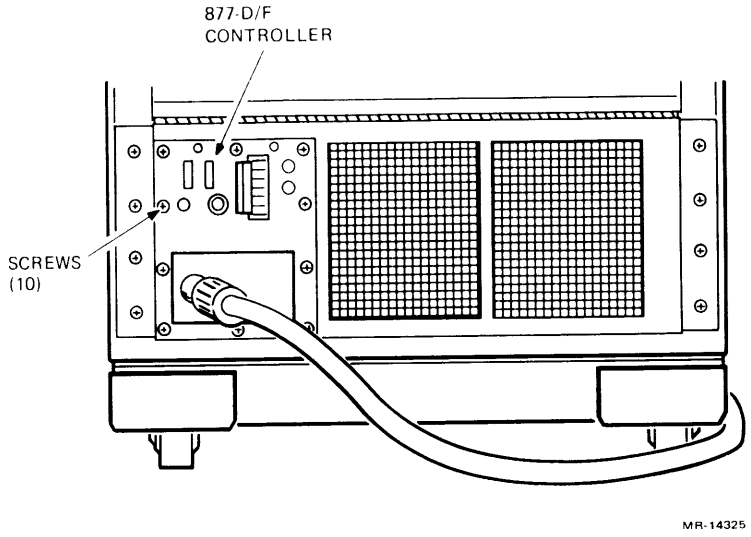

Figure 3-14 Power Controller Removal – Rear View

8. Grasp the controller's metal power cord restraint and remove the controller from the cabinet rear.

This completes the removal procedure for the power controller. To reinstall the controller reverse the above procedure.

3.10 SLU INTERFACE ASSEMBLY REMOVAL/REPLACEMENT

Both products contain an SLU interface assembly, but use different removal and replacement procedures.

3.10.1 Cabinet SLU Assembly Removal

To remove the SLU assembly use the following procedure.

1. Open the front and rear doors using the hex key.
2. Turn off the power supply and power controller circuit breakers.
3. Remove the ac power cord from the outlet.
4. Loosen the ten captive screws securing the bulkhead to the frame.
5. Open the bulkhead by pulling down from the top.
6. Unplug the SLU cable (console terminal) from the connector.
7. Loosen and remove the two hex standoffs securing the connector to the cross member.
8. Unplug the cable from the SLU assembly connector (Figure 3-15).

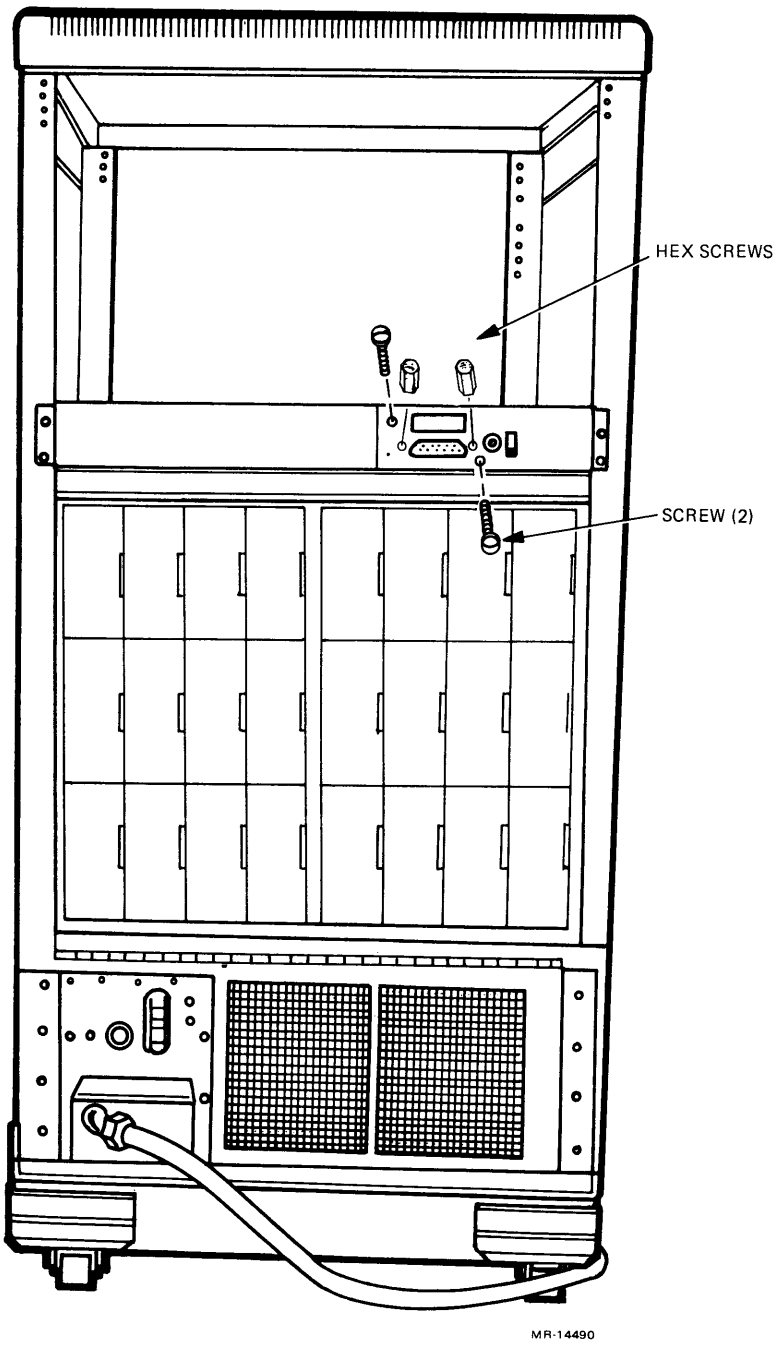

Figure 3-15 Cabinet SLU Assembly Removal

9. Hold the SLU assembly while removing the two screws that secure the SLU assembly to the crossmember.

10. Remove the SLU assembly from the cabinet.

This completes the removal of the SLU assembly. To reinstall the SLU assembly reverse the above procedure.

3.10.2 Box SLU Assembly Removal/Replacement

To remove the SLU assembly, use the following procedure.

1. Turn off the circuit breaker.
2. Unplug the ac power cord from the outlet.
3. Remove the cable plugged into the SLU connector.
4. Remove the two hex standoffs securing the connector to the back panel.
5. Remove the four screws on the top cover, and remove the cover.
6. Remove the connector plugged into the SLU assembly board.
7. Remove the two assembly mounting screws from the rear of the box (Figure 3-16).

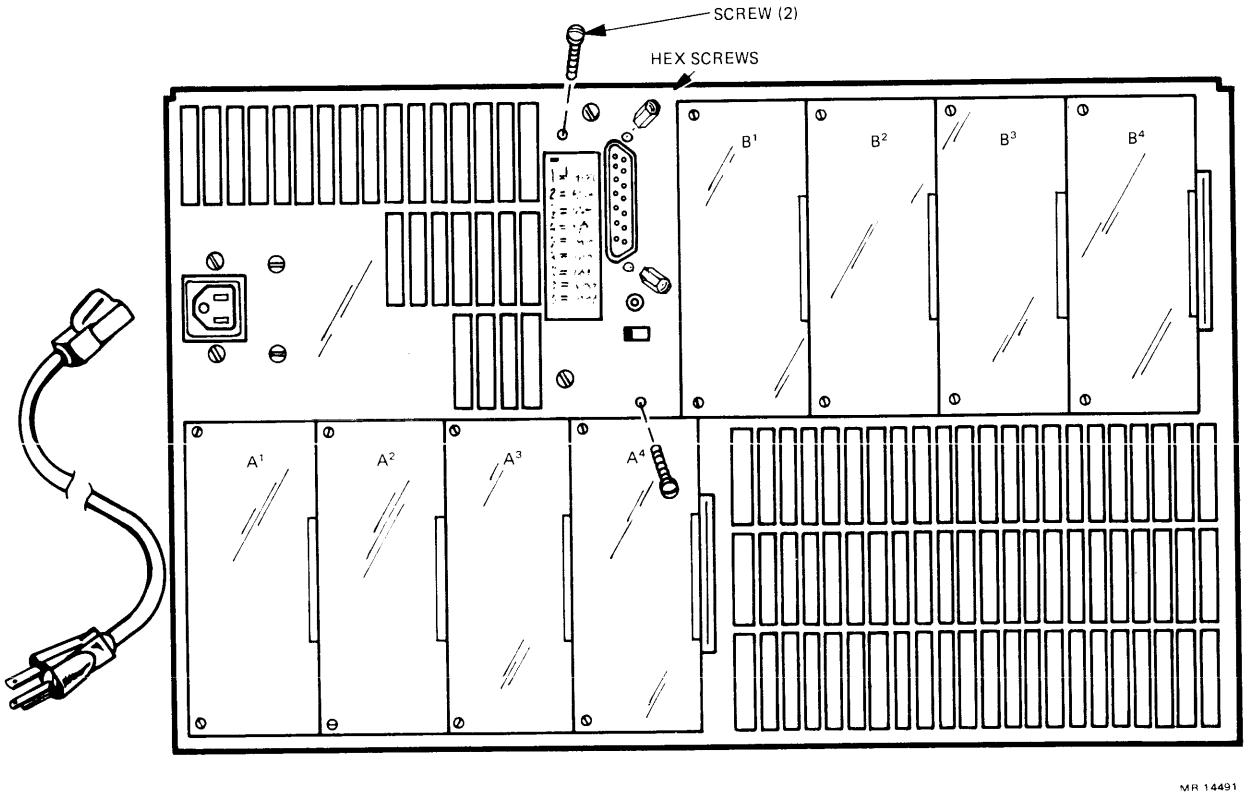

Figure 3-16 Box SLU Assembly Removal

8. Remove the hex standoffs from the SLU connectors.
9. Remove the SLU assembly from the box.

This completes the removal of the SLU assembly. To reinstall the assembly reverse the above procedure.

3.11 CPU BACKPLANE REMOVAL/REPLACEMENT

Depending on the number of options installed in the system, a backplane replacement can be a time-consuming task. It is recommended that you replace the backplane only if it is clearly known to be the faulty FRU.

3.11.1 Cabinet Backplane Removal

To remove the CPU backplane, use the following procedure.

1. Open the front and rear doors using the hex key.
2. Turn off the power supply and power controller circuit breakers.
3. Remove the ac power cord from the outlet.

NOTE

If the system contains a BBU, it must be removed. Perform steps 4 thru 10 of the BBU removal procedure (subsection 3.11).

4. Remove and label all the module cables.
5. Remove all cabinet modules and label each with its backplane slot number.
6. Remove the right side panel (Figure 3-17).

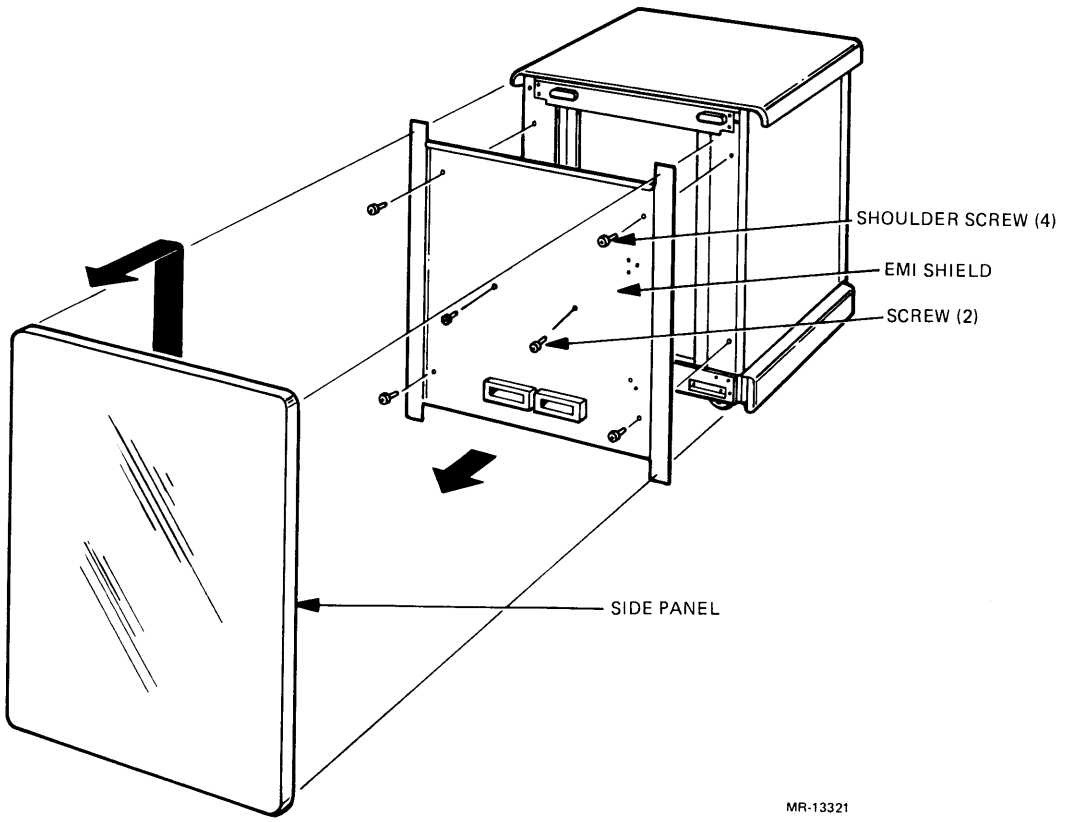

Figure 3-17 Side Panel Removal

7. Remove the two Phillips-head and four shoulder screws securing the EMI panel to the cabinet frame.

8. Remove the left side panel.

9. Remove the four shoulder screws securing the EMI panel to the cabinet frame.

10. Loosen the ten screws securing the bulkhead to the cabinet frame and lower the bulkhead (Figure 3-18).

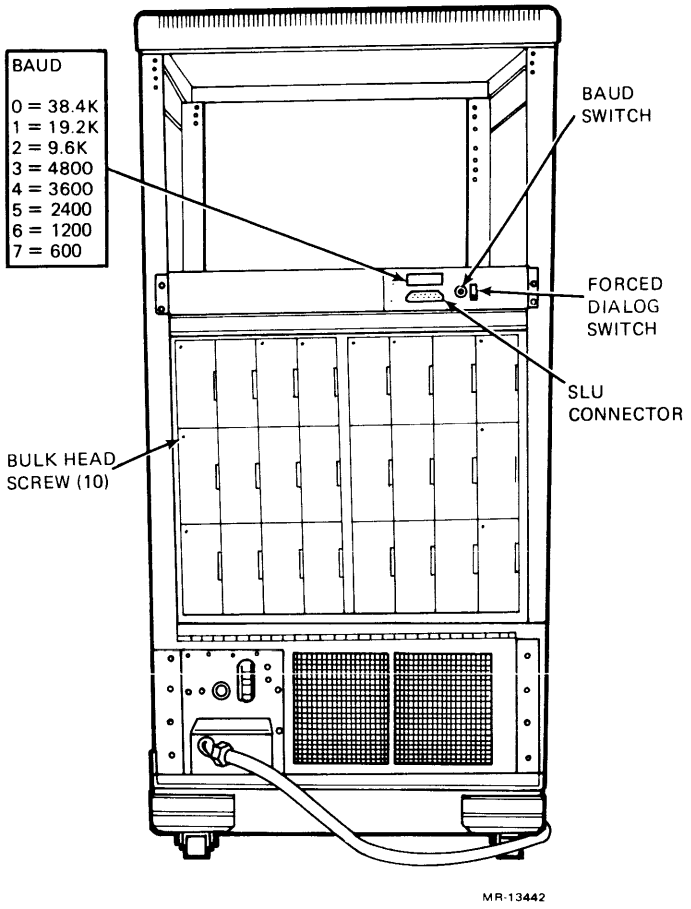

Figure 3-18 Cabinet Rear View

11. Remove the four black plastic retainers securing the plastic lexan cover over the space for the expansion backplane location (Figure 3-19).

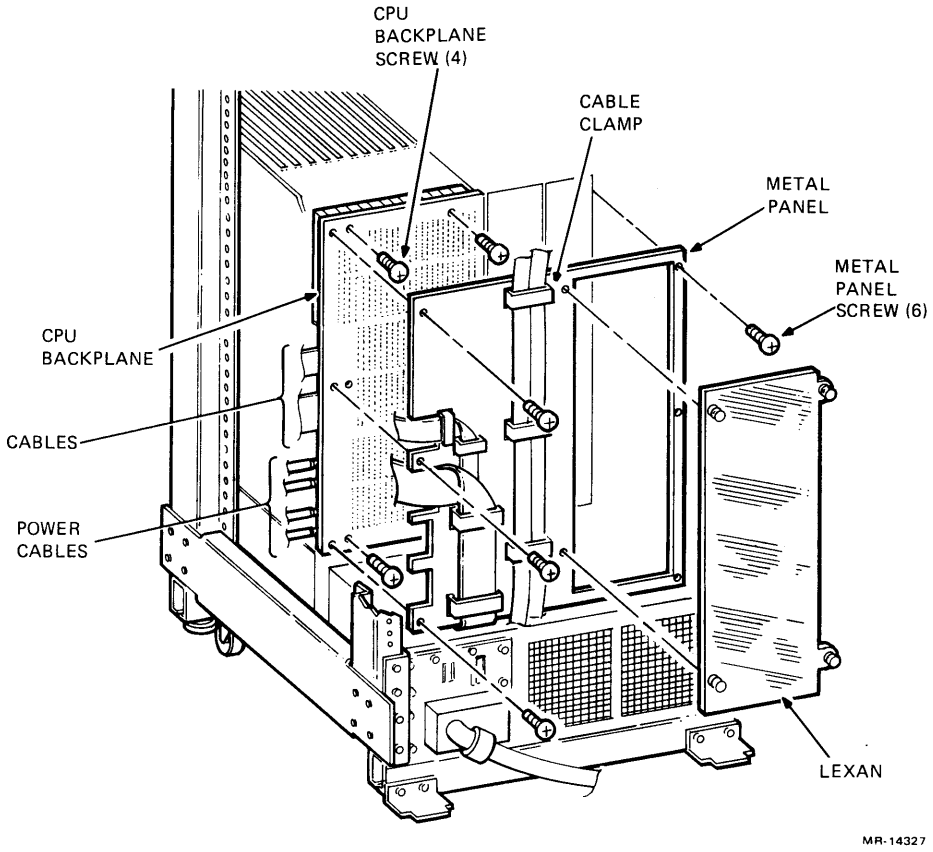

Figure 3-19 Cabinet Backplane Removal

12. If an expansion backplane is installed, remove the power connectors. Remove the lexan cover through the left side cabinet access.

13. Disconnect the power cables for the expansion backplane.

14. Loosen the cable clamps on the metal panel covering the rear access to the backplane.

15. Remove the six screws securing the metal panel over the rear access to the backplane. Remove the metal panel.

16. Remove the four flathead screws securing the backplane to the card cage.

17. Remove the backplane by pulling the it toward the cabinet rear and twisting it through the side panel access.

This completes the removal procedure for the backplane. To reinstall the backplane reverse the above procedure.

3.11.2 Box Backplane Removal/Replacement

To remove the backplane, use the following procedure.

1. Turn off the power circuit breaker.
2. Unplug the ac power cord from the outlet.
3. Remove the screws securing the top cover, and remove the cover.
4. Unplug all the module cables and label each with its module number.
5. Unplug all the modules. Label each module with its slot number.
6. Remove the four 1/4-inch nuts securing the four power cables. Unplug the two backplane cables (Figure 3-20).

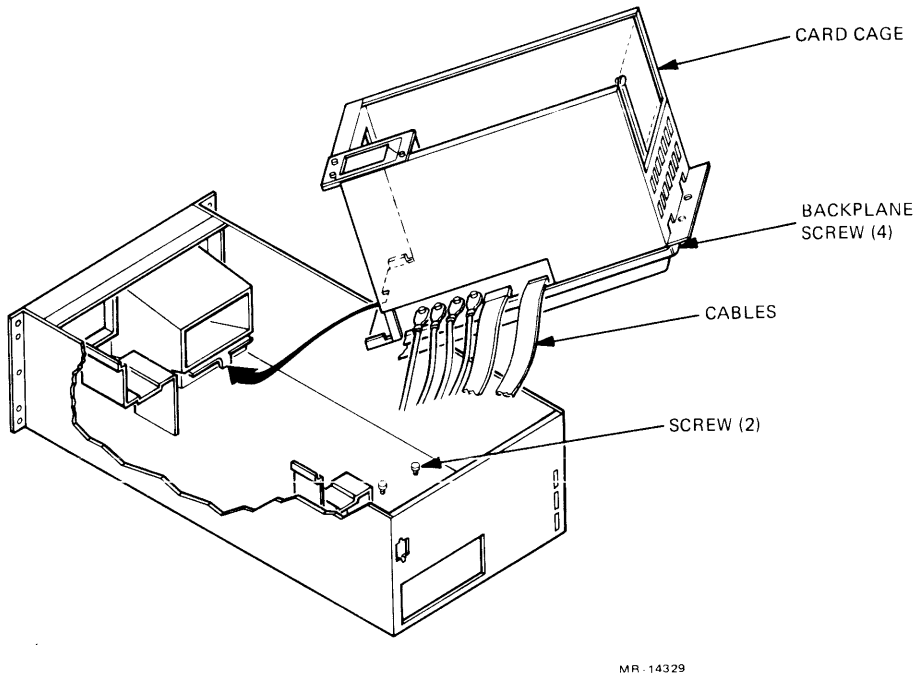

Figure 3-20 Box Backplane Removal

7. Remove the two screws located at the rear of the card cage.
8. Slide the card cage to the rear of the box. Lift and slide the card cage to the rear and remove from the box.
9. Turn the card cage over and remove the four backplane mounting screws. Remove the backplane.

This completes the removal procedure for the CPU backplane. To reinstall the backplane reverse the above procedure.

3.12 CABINET BBU REMOVAL/REPLACEMENT

To remove the BBU use the following procedure.

1. Open the front and rear doors using the hex key.
2. Turn off the power supply and power controller circuit breakers.
3. Unplug the ac power cord from the outlet.
4. Remove the cabinet right side panel by lifting it straight up from both sides. Be careful—the panel is heavy (Figure 3-21).

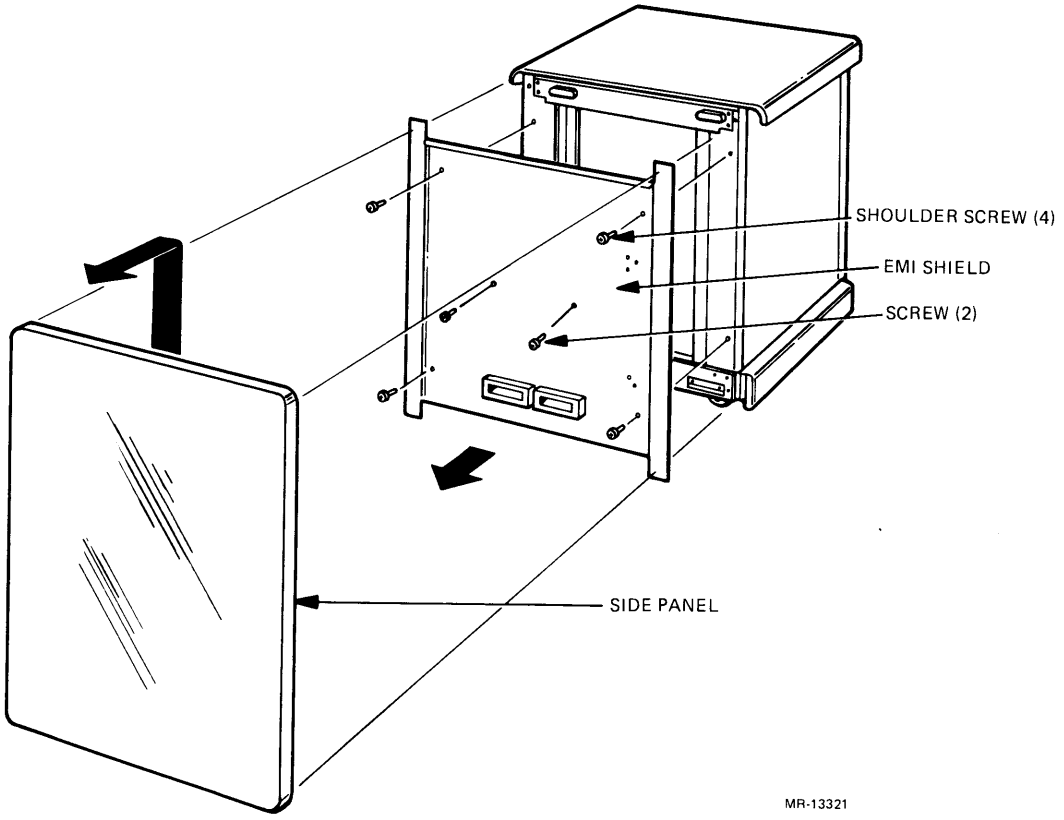

Figure 3-21 Side Panel Removal

5. Remove the two Phillips-head and four shoulder screws securing the EMI panel attached to the cabinet frame. Remove the shield.
6. Loosen and remove the ground wires attached to the two BBU rear panel studs.
7. Carefully unplug the three cables attached to connectors on the BBU rear panel.
8. Unplug the BBU power cord from the rear panel.

CAUTION
The weight of the BBU is 19 kg (42 lbs); lifting and positioning the BBU requires two people.

9. Loosen and remove the four hex nuts securing the BBU to the cabinet frame (Figure 3-22).

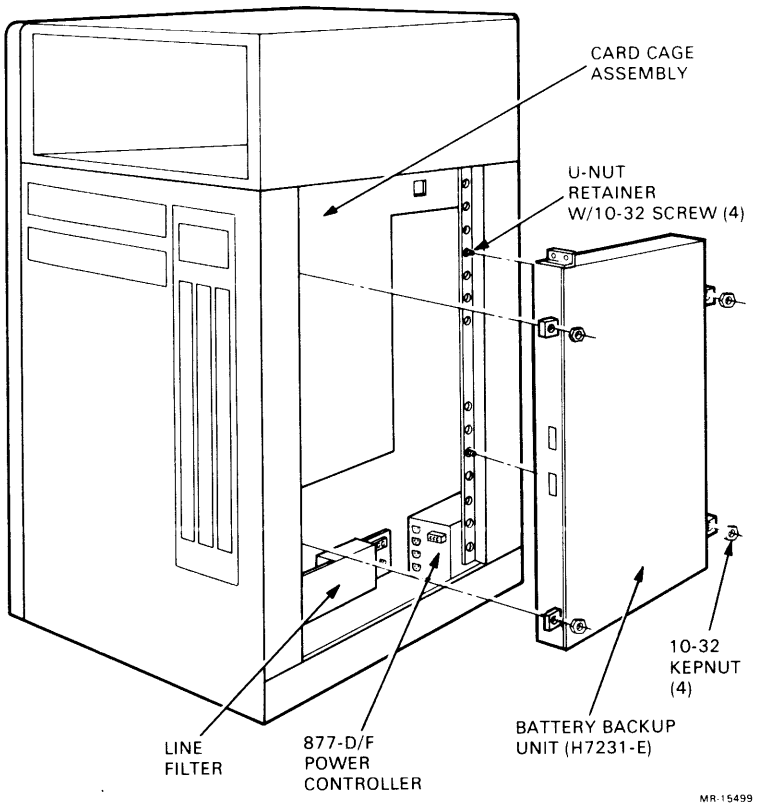

Figure 3-22 BBU Removal

10. Slide the BBU outward from the frame, and off of the mounting screws.

This completes the removal procedure for the BBU. To reinstall the BBU, reverse the procedure.

3.13 BOX BBU REMOVAL/REPLACEMENT

To remove the BBU from the box system complete the following procedure.

1. Turn off the box power supply circuit breaker (Figure 3-23).

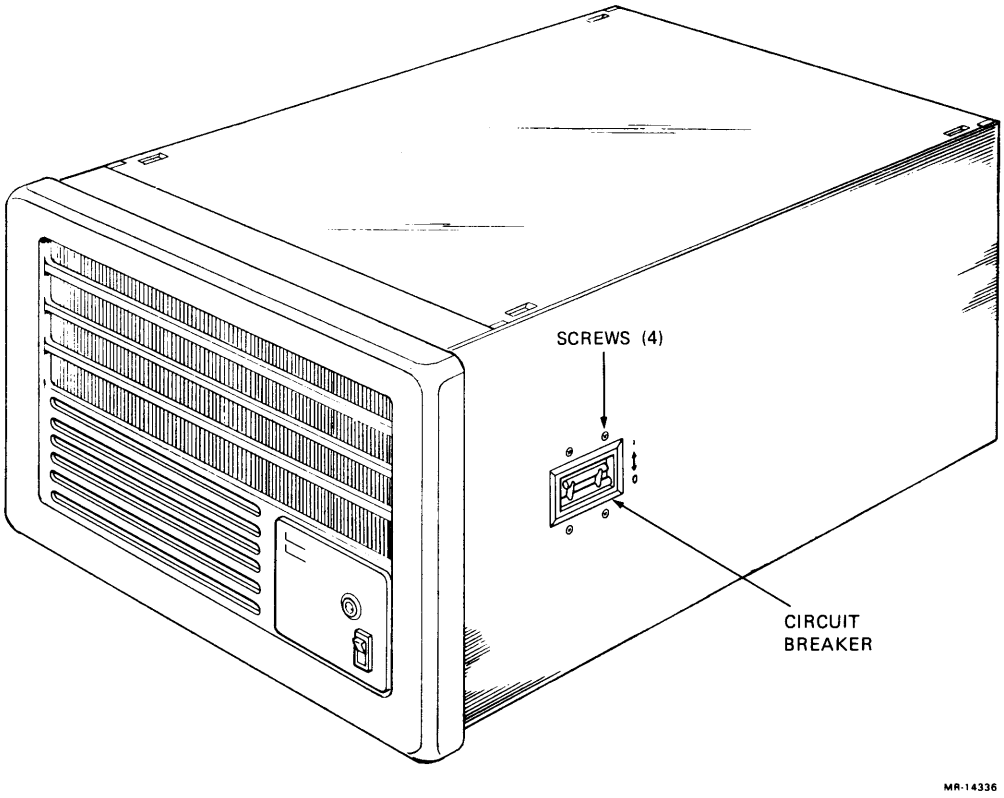

Figure 3-23 Box Circuit Breaker Location

2. Unplug both the box and BBU from the ac power outlet.

3. Loosen and remove both ground hex nuts located on the BBU bulkhead panel (Figure 3-24).

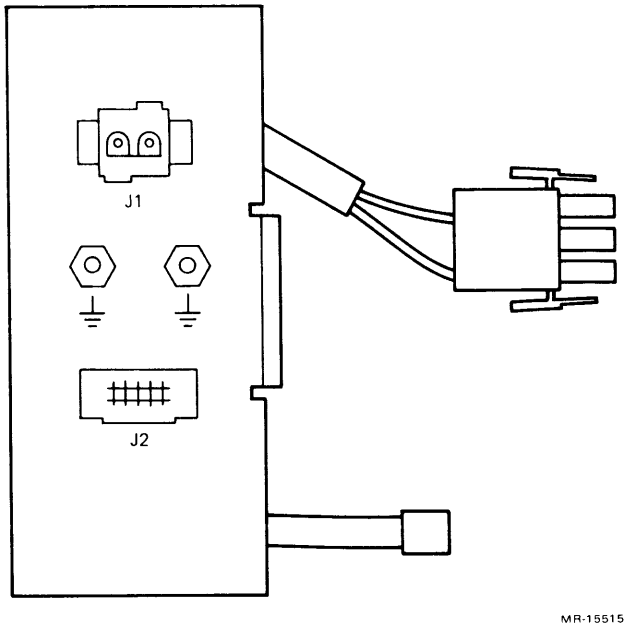

Figure 3-24 BBU Bulkhead Panel

4. Unplug both connectors J1 and J2 located on the box BBU bulkhead panel.

CAUTION
The weight of the BBU is 19 kg (42 lbs); lifting and positioning the unit requires two people.

5. Follow the rack manufacturer's directions for removing the BBU from the rack assembly.

This completes the removal of the BBU. To reinstall the BBU reverse the procedure.

3.14 CABINET PERIPHERAL ACCESS

Always extend the front stabilizer bar before sliding an option out of the top portion of the cabinet. The bar keeps the cabinet from tipping forward (Figure 3-25).

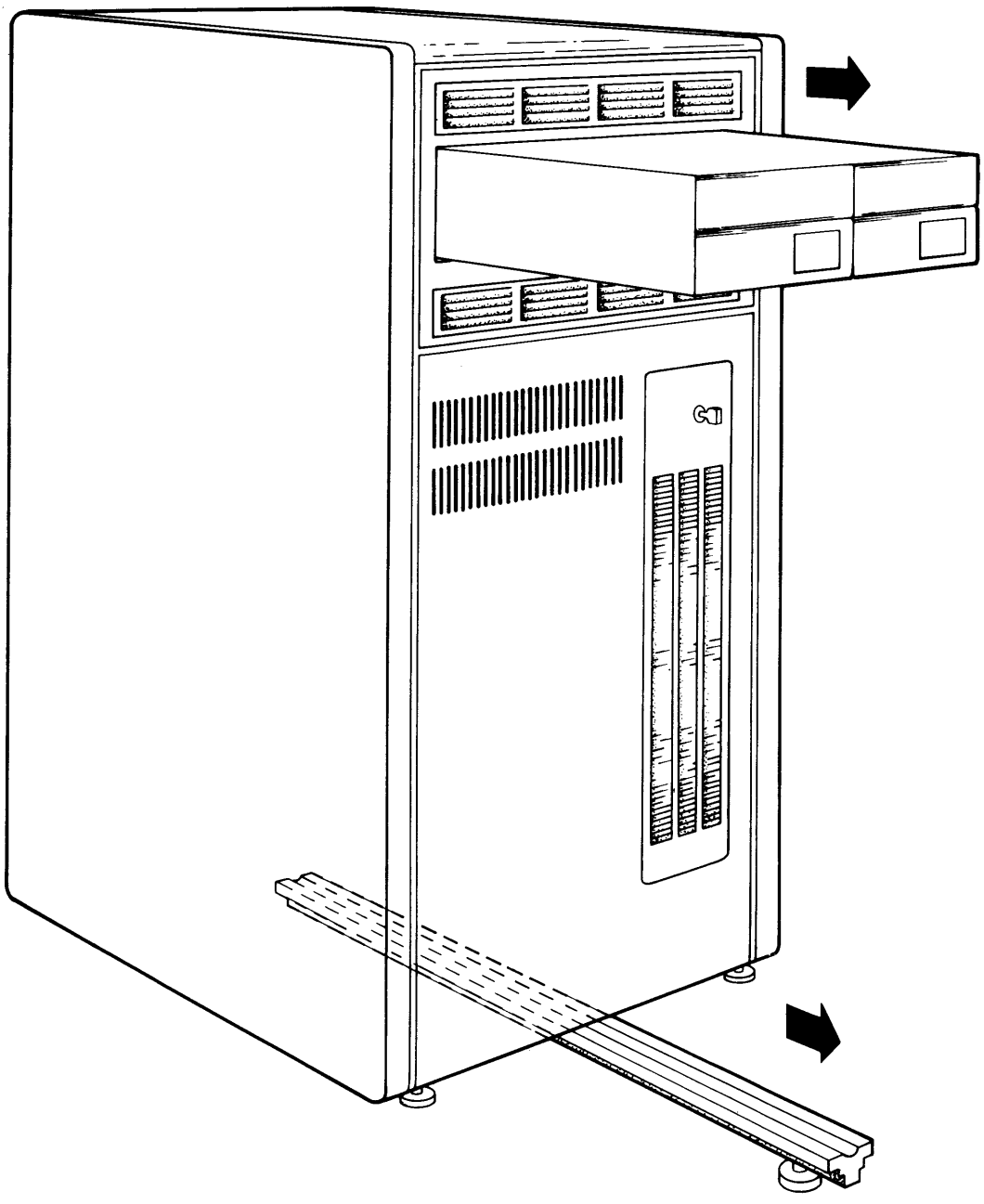

Figure 3-25 Stabilizer Bar Extension

CHAPTER 4
SYSTEM REGISTER DESCRIPTIONS

4.1 PAGE ADDRESS REGISTERS (PAR)

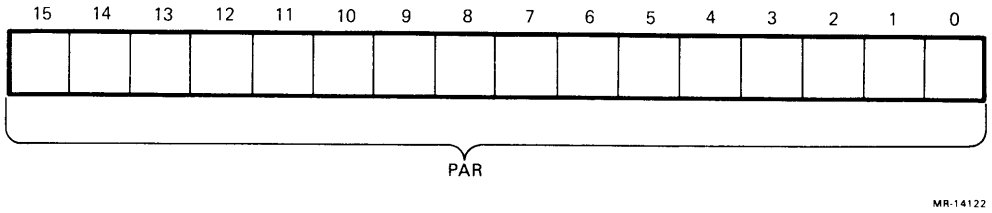

Figure 4-1 Page Address Register Format

4.2 PAGE DESCRIPTOR REGISTERS (PDR)

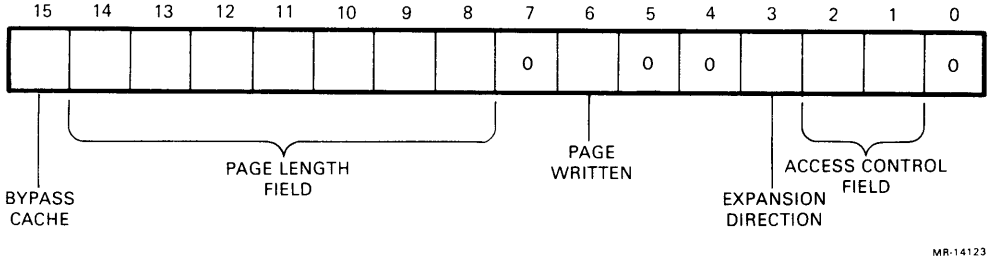

Figure 4-2 Page Descriptor Register Format

Table 4-1 Page Descriptor Register Bit Descriptions

Bit	Name	Function
15	Bypass cache (R/W)	This bit implements a conditional cache bypass mechanism. If set, references to the selected virtual page will bypass the cache. A cache bypass causes the cache location to be invalidated whenever a read or write hit occurs.
14:8	Page length field (R/W)	This field specifies the block number which defines the boundary of the current page. The block number of the virtual address is compared against the page length field to detect length errors. An error occurs when expanding upwards if the block number is greater than the page length field, and when expanding down if the block number is less than the page length field.
6	Page written (RO)	This bit indicates whether or not this page has been modified (i.e. written into) since either the PAR or PDR was loaded (1 is affirmative). It is useful in applications which involve disk swapping and memory overlays. It is used to determine which pages have been modified and must be saved, and which pages have not been modified and can be overlaid. This bit is reset to 0 whenever either the PDR or the associated PAR is written into.
3	Expansion direction (R/W)	This bit specifies in which direction the page expands. If ED=0, the page expands upwards from block number 0 to include blocks with higher addresses; if ED=1, the page expands downwards from block number 127 to include blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space.
2:1	Access control	This field contains the access rights to this particular page. The access codes or "keys" specify the manner in which a page may be accessed and whether or not a given access should result in an abort to the current operation. The access codes are: 00 Non-resident – abort all accesses 01 Read only – abort on writes 10 Not used – abort all accesses 11 Read/write

4.3 MEMORY MANAGEMENT REGISTER 0

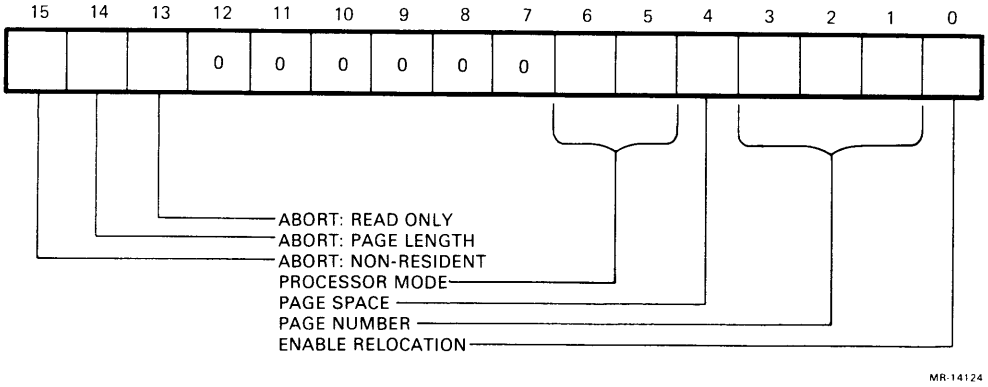

Figure 4-3 Memory Management Register 0 Format

Table 4-2 Memory Management Register 0 Bit Descriptions

Bit	Name	Function
15	Abort - nonresident (R/W)	Bit <15> is set by attempting to access a page with an access control field key equal to 0 or 2. It is also set by attempting to use memory relocation with a mode (PS<15:14>) of 2.
14	Abort - page length (R/W)	This bit is set by attempting to access a location in a page with a block number (virtual address bits <12:6>) that is outside the area authorized by the page length field of the PDR for that page.
13	Abort - read only (R/W)	This bit is set by attempting to write in a "read only" page. "Read-only" pages have access keys of 1.

NOTE

Bits <15:13> can be set by an explicit write; however, such an action does not cause an abort. Whether set explicitly or by an abort, bits <15:13> cause memory management to freeze the contents of MMR0 <6:1>, MMR1, and MMR2. The status registers remain frozen until MMR0 <15:13> are cleared by an explict write or any initialization sequence.

Table 4-2 Memory Management Register 0 Bit Descriptions (Cont.)

Bit	Name	Function
6:5	Processor mode (R/W)	These bits indicate the processor mode (kernel/supervisor/user/illegal) associated with the page causing the abort (kernel = 00, supervisor = 01, user = 11, illegal = 10). If the illegal mode is specified, an abort is generated and bit <15> is set.
4	Page space (RO)	This bit indicates the address space (I or D) associated with the page causing the abort (0 = I space, 1 = D space).
3:1	Page number (RO)	These three bits contain the page number of the page causing the abort.
0	Enable relocation (R/W)	This bit allows address relocation. When set to 1, all addresses are relocated. When bit 0 is set to 0, memory management is inoperative and addresses are not relocated.

4.4 MEMORY MANAGEMENT REGISTER 1

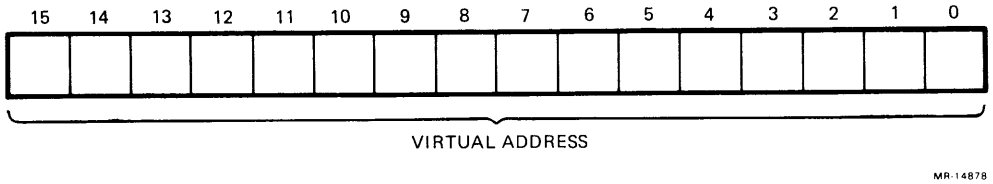

Figure 4-4 Memory Management Register 1 Format

4.5 MEMORY MANAGEMENT REGISTER 2 (Address 17 777 576)

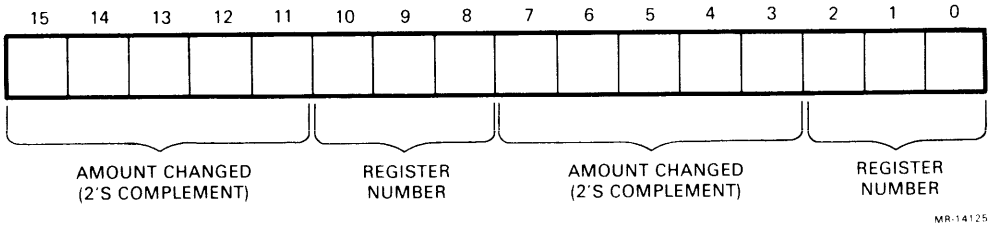

Figure 4-5 Memory Management Register 2 Format

4.6 MEMORY MANAGEMENT REGISTER 3 (Address 17 777 xxx)

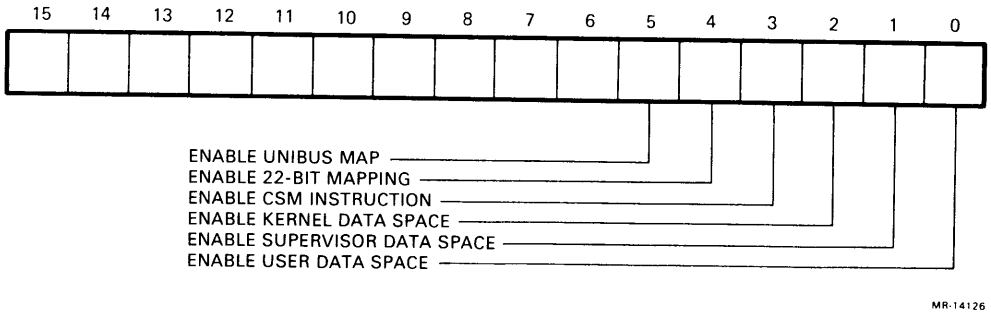

Figure 4-6 Memory Management Register 3 Format

Table 4-3 Memory Management Register 3 Bit Descriptions

Bit(s)	Name	Function
15:06	Unused	Reserved for future use.
5	Enable UNIBUS map (R/W)	This bit enables the I/O map for the UNIBUS adapter.
4	Enable 22-bit mapping (R/W)	This bit, when set, selects 22-bit memory addressing. When this bit is clear, 18-bit addressing is selected (18- or 22-bit addressing is actually enabled only when MMR0 bit 0 is set).
3	Enable CSM instruction (R/W)	This bit enables recognition of the call supervisor mode (CSM) instruction.
2:0	Enable data space (R/W)	These three bits enable data space mapping for kernel, supervisor, and user mode, respectively.

4.7 KDJ11-B CACHE REGISTERS - DATA ORGANIZATION

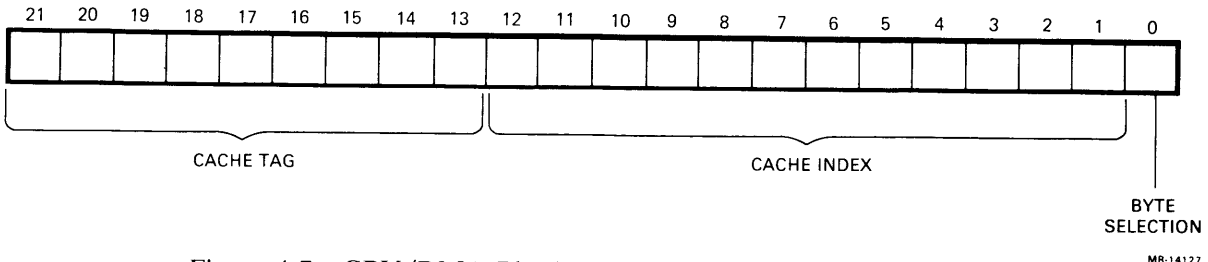

Figure 4-7 CPU/DMA Physical Address Interpretation Register

Table 4-4 CPU/DMA Physical Address Interpretation Bit Descriptions

Bit(s)	Name	Function
21:13	Cache tag (R/W)	1. During CPU read/write operations, these bits are compared with bits 21:13 of the CPU cache tag register (Figure 4-8) to determine the cache hit/miss status. 2. During DMA read/write operations, these bits are compared with bits 21:13 of the DMA tag register (Figure 4-9) to determine the cache hit/miss status. For either CPU or DMA operations, a tag hit occurs when the cache tag contents matches the CPU/DMA tag register and the CPU/DMA valid bit is set.
12:01	Cache index (R/W)	The CPU cache interprets the CPU/DMA physical address directly and selects one of 4096 word cache memory locations.
00	Byte selection	During CPU/DMA write operations, setting this bit selects writing into the high-byte cache memory location (Figure 4-10).

The high-byte parity bit reflects odd parity on data bits <15:08>.

The low-byte parity bit reflects even parity on data bits <07:00>.

The CPU tag parity bit reflects odd parity on CPU tag bits <21:13>.

The DMA tag parity bit reflects odd parity on DMA tag bits <21:13>.

The CPU and DMA tag valid bits are not included in the CPU and DMA tag parity calculations.

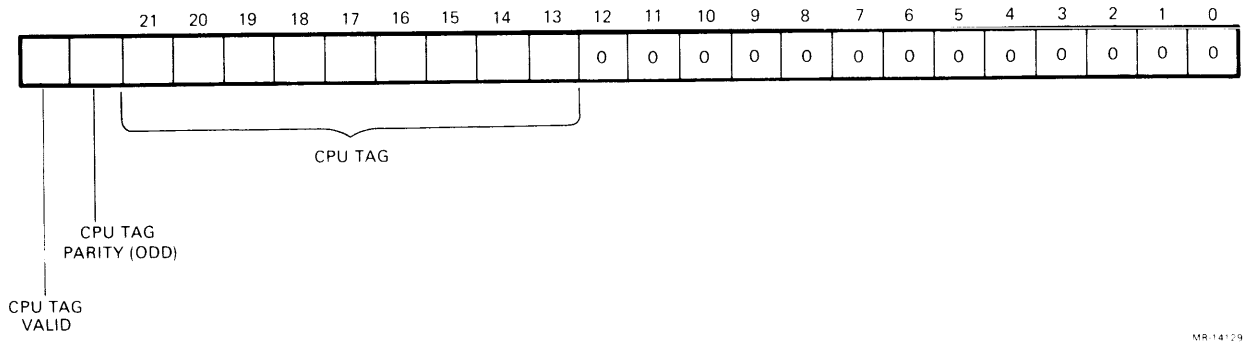

Figure 4-8 CPU Cache Tag Register Format

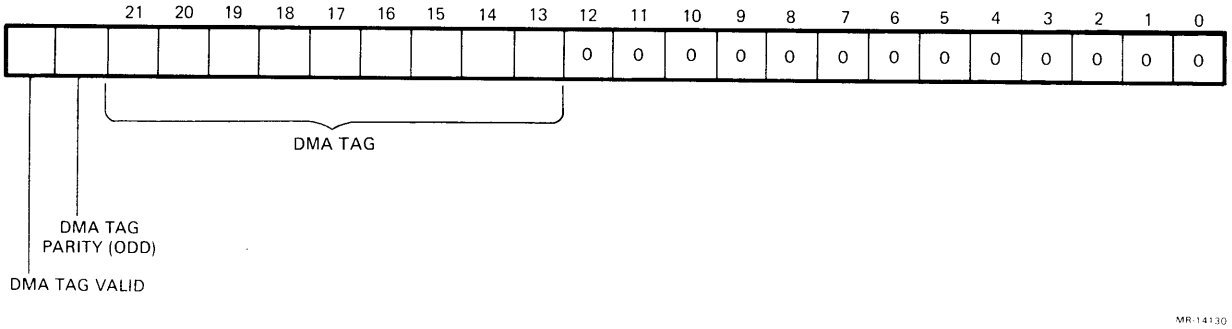

Figure 4-9 DMA Tag Register Format

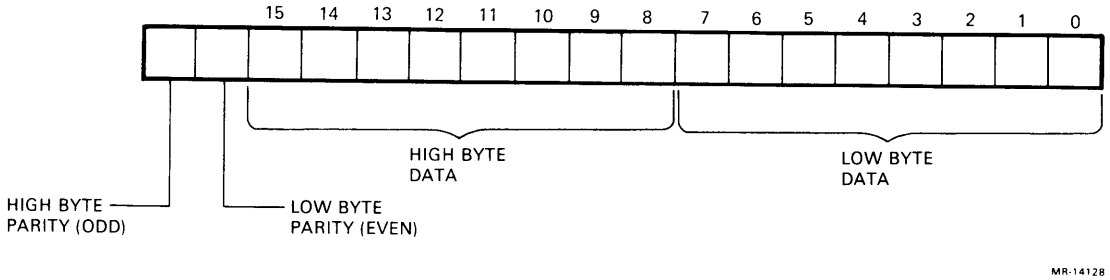

Figure 4-10 CPU Cache Data Organization

4.8 CACHE CONTROL REGISTER (Address 17 777 746)

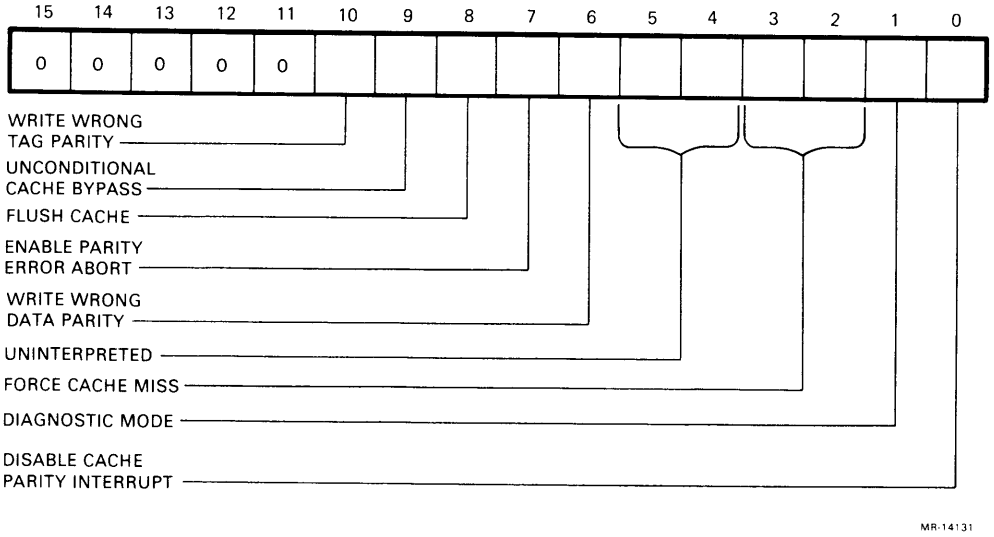

Figure 4-11 Cache Control Register (CCR) Format

Table 4-5 Cache Control Register Bit Descriptions

Bit(s)	Name	Function
15:11	—	Unused, always read as cleared bits.
10	Write wrong tag parity (R/W)	When this bit is set, the CPU and DMA Tag Parity bits are both written as wrong parity during all operations which update these bits. A cache tag parity error will thus occur on the next access to that location.
09	Unconditional cache bypass (R/W)	When this bit is set, all references to memory by the CPU will bypass the cache and go directly to main memory. Read or write hits will result in the invalidation of the corresponding cache location; misses will not affect the cache contents.
08	Flush cache (WO)	Writing a "1" into this bit clears all CPU tag and DMA tag valid bits invalidating the entire contents of the cache. Writing a "0" into this bit has no effect. Flush cache always reads as zero. The KDJ11-B requires approximately 1 ms to flush the cache. During the period, DMA activity is possible and CPU activity is suspended.
07	Parity error abort (R/W)	This bit is set for diagnostic purposes only. When it is set, a cache parity error (during a CPU cache read) will cause the CPU to abort the current instruction and trap to parity error vector 114. When this bit is clear, a cache parity error (during a CPU cache read) results in a force miss and data fetch from main memory. The CPU will trap to 114 only if CCR bit <0> is clear. DMA cycle cache parity errors will cause a trap to 114 if CCR <7> is set or if CCR <0> is clear. CCR <7> has no effect on main memory parity errors which always cause the CPU to abort the current instruction and trap to 114.
06	Write wrong data parity (R/W)	When this bit is set, both the high and low data parity bits are written with wrong parity during all operations which update these bits. This will cause a cache data parity error to occur on the next access to that location.
03:02	Force miss (R/W)	When either of these bits is set, CPU reads will be reported as cache misses.
01	Diagnostic mode (R/W)	When this bit is set, a 10 μs nonexistent memory timeout during a word write will not cause a nonexistent memory trap and will not set CPU error register bit 05. All nonbypass and nonforced miss word writes will allocate the cache regardless of the nonexistent memory timeout.
00	Disable cache parity interrupt (R/W)	This bit controls cache parity interrupts when CCR <7> is clear (normal operation). If CCR <7> is clear, a cache parity error (during a CPU cache read) results in a force miss and data fetch from main memory. The CPU will trap to 114 only if CCR bit <0> is clear. DMA cycle cache parity errors will cause a trap to 114 if CCR <7> is set, or if CCR <0> is clear.

Table 4-6 summarizes the effect of CCR <7,0> on parity errors during CPU cache reads.

Table 4-6 Cache Parity Errors During CPU Cycles

CCR<7>	CCR<0>	Result of Cache Parity Error
0	0	Cache miss and update cache; interrupt to 114.
0	1	Cache miss and update cache; no interrupt.
1	X	Abort instruction and trap to 114.

Table 4-7 summarizes the effect of CCR <7,0> on DMA tag parity errors during DMA writes.

Table 4-7 Cache Parity Errors During DMA Cycles

CCR<7>	CCR<0>	Result of Cache Parity Error
0	0	Interrupt to 114.
0	1	No interrupt.
1	X	Trap to 114.

4.9 MEMORY SYSTEM ERROR REGISTER (Address 17 777 744)

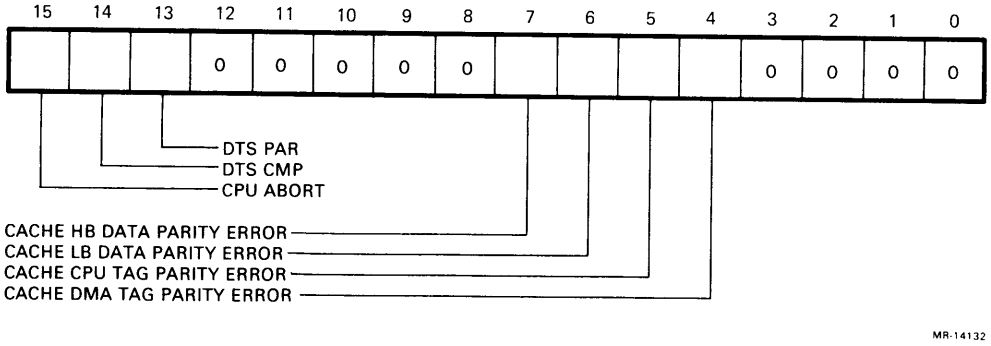

Figure 4-12 Memory System Error Register (MSER) Format

Table 4-8 Memory System Error Register Bit Descriptions

Bit(s)	Name	Function
15	CPU abort (RO)	This bit is set if a cache or main memory parity error results in an instruction abort (i.e., only during the demand read cycle). Cache parity errors cause an abort only if CCR <7> is set. Main memory parity errors always cause an abort.
14	DMA tag store comparator (DTS CMP) (RO)	In standalone mode (BCSR <8> set), this bit indicates the output of the cache DMA tag store comparator for the previous non-I/O page reference with cache miss. When BCSR <8> is clear, DTS CMP reads as a "0".
13	DMA tag store parity (DTS PAR) (RO)	In standalone mode (BCSR <8> set), this bit indicates the output of the DMA tag store parity check logic for the previous non-I/O page reference with cache miss. When BCSR <8> is clear, DTS PAR reads as a "0".
12-08	Unused	These bits always read as "0".
07	Cache HB data parity error (R/W)	This bit is set if a parity error is detected in the high-data byte during a CPU cache read. If CCR <7> is clear, MSER <7> is also set by a low-byte parity error and by the set condition of MSER <5> or <4>.
06	Cache LB data parity error (RO)	This bit is set if a parity error is detected in the low-data byte during a CPU cache read. If CCR <7> is clear, MSER <6> is also set by a high-byte parity error and by the set condition MSER bits <5> or <4>.
05	Cache CPU tag parity error (RO)	This bit is set if a parity error is detected in the CPU tag field during a CPU cache read. If CCR <7> is clear, MSER <7> is also set by a high- or low-data byte parity error.
		NOTE **Cache parity errors are ignored (do not affect MSER <7-5>), if either CCR <3> or <2> (force miss) is set, or if the CPU tag valid bit is clear.**
04	Cache DMA tag parity error (RO)	This bit is set if a parity error is detected in the DMA tag field during a DMA write
		NOTE **Cache parity errors are ignored (do not affect MSER <4>), if either CCR <3> or <2> (force miss) is set, or if the DMA tag valid bit is clear.**
03:00	Unused	These bits always read as "0".

Main memory parity errors always cause the CPU to abort the current instruction, to set MSER <15> and to trap through vector location 114.

Cache parity errors which occur during a CPU cache access may result in an instruction abort and/or a trap to location 114, depending on the following condition of CCR bits <7> and <0>:

1. If CCR <7> (parity error abort) is set, a cache parity error causes the CPU to abort the current instruction, to set MSER <15> and the relevant error bit(s) MSER <7:5>, and to trap through vector location 114.

2. If CCR <7> is clear, and if CCR <0> is also clear, a cache parity error causes the CPU to force a cache miss, set the relevant error bits MSER <7:5>, and to trap through vector location 114.

3. If CCR <7> is clear, and if CCR <0> is set, a cache parity error causes the CPU to force a cache miss and to set the relevant error bits MSER <7:5>. The CPU does not trap through vector location 114.

Cache DMA tag field parity errors which occur during a DMA cycle cause a trap to location 114 if CCR <7> is set, or if CCR <0> is clear.

The MSER is cleared by any MSER write reference. It is also cleared on power-up or by a console start. It is unaffected by a reset instruction.

4.10 HIT/MISS REGISTER (Address 17 777 752)

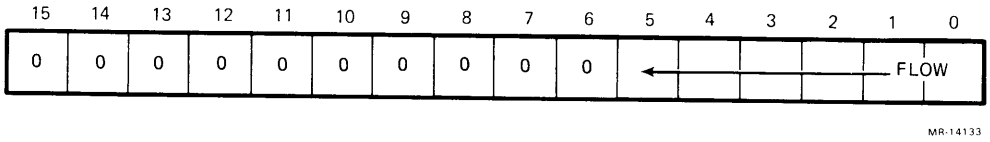

Figure 4-13 Hit/Miss Register Format

Table 4-9 Hit/Miss Register Bit Descriptions

Bit	Name	Function
15:06	Unused	Always read as zeros.
05:00	Cache hit	Bits enter from the right (at bit <0>) and are shifted left. A set bit indicates a cache hit, a cleared bit indicates a cache miss.

4.11 PROCESSOR STATUS WORD (Address 17 777 776)

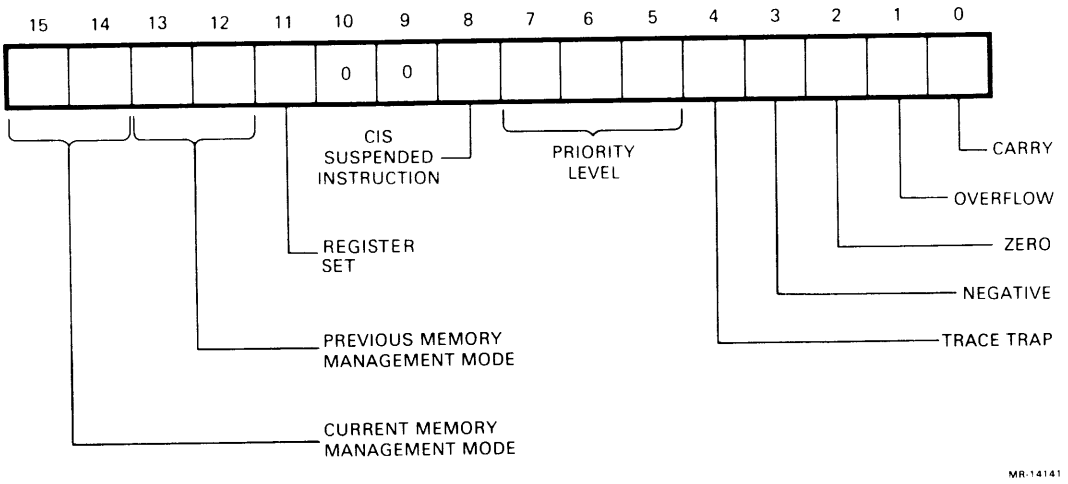

Figure 4-14 Processor Status Word Register (PSW)

Table 4-10 Processor Status Word Bit Descriptions

Bit	Name	Function
15:14	Current mode (R/W, protected)	Current processor mode: 00 = kernel 01 = supervisor 10 = illegal (traps) 11 = user
13:12	Previous mode (R/W, protected)	Previous processor mode, same encoding as current mode.
11	Register set (R/W, protected)	General register set select: 0 = register set 0 1 = register set 1
8	Suspended instruction (R/W)	Reserved for future use.
7:5	Priority (R/W, protected)	Processor interrupt priority level.
4	Trace trap (R/W, protected)	Set to force a trace trap.
3:0	Condition codes (R/W)	Processor condition codes.

4.12 PROGRAM INTERRUPT REQUEST REGISTER (Address 17 777 772)

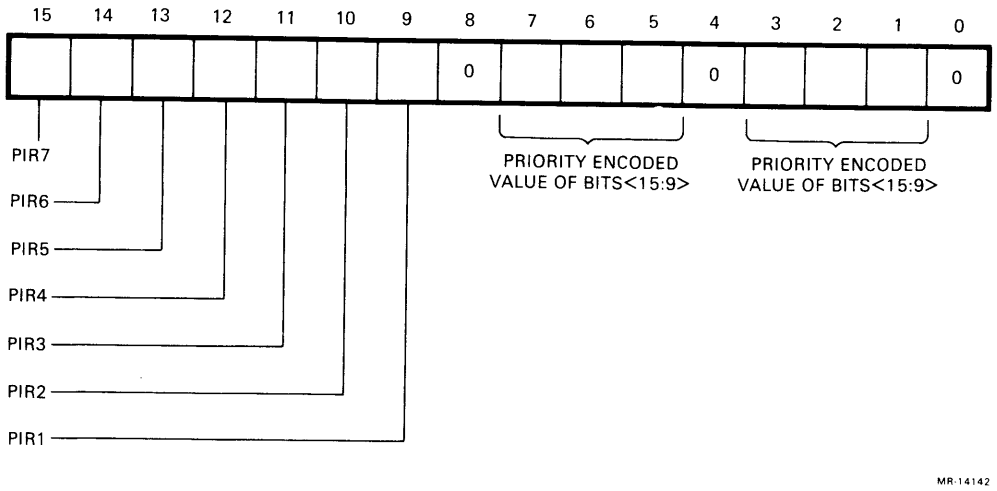

Figure 4-15 Program Interrupt Request (PIR) Register

Table 4-11 Program Interrupt Request Register Bit Descriptions

Bit(s)	Name	Function
15:09	PIR 7-1	Each bit, when set, provides one of seven levels of software interrupt corresponding to interrupt priority levels 7 through 1.
08		Unused.
07:05	Priority encoded value of bits <15:09>	These three bits are set by the CPU to the encoded value of the highest pending interrupt request (bits 15:09).
04		Unused.
03:00	Priority encoded value of bits <15:09>	The function of these bits is identical to bits 07:05.

4.13 CPU ERROR REGISTER (Address 17 777 766)

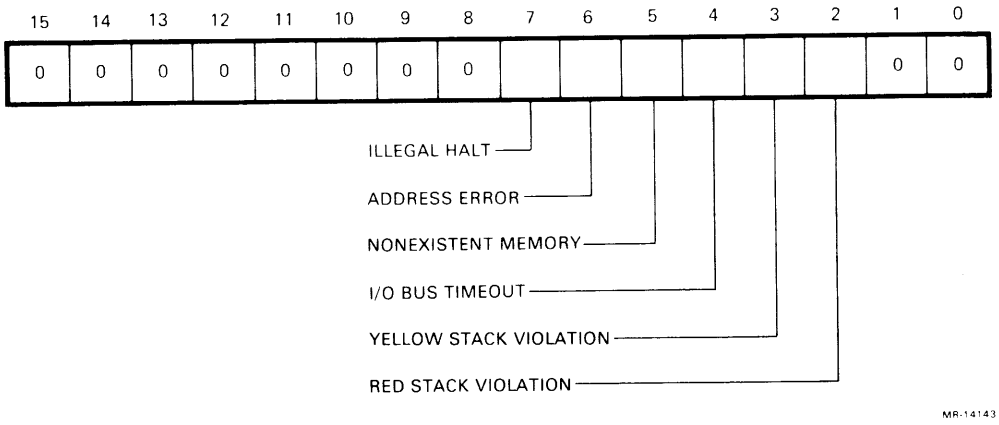

Figure 4-16 CPU Error Register Format

Table 4-12 CPU Error Register Bit Descriptions

Bit	Name	Function
7	Illegal halt	Set when execution of a halt instruction is attempted in user or supervisor mode.
6	Address error (RO)	Set when word access to an odd byte address or an instruction fetch from an internal register is attempted.
5	Nonexistent memory (RO)	Set when a reference to main memory times out.
4	I/O bus timeout (RO)	Set when a reference to the I/O page times out.
3	Yellow stack violation (RO)	Set on a yellow zone stack overflow trap.
2	Red stack violation (RO)	Set on a red zone stack overflow trap.

4.14 CONFIGURATION AND DISPLAY REGISTER

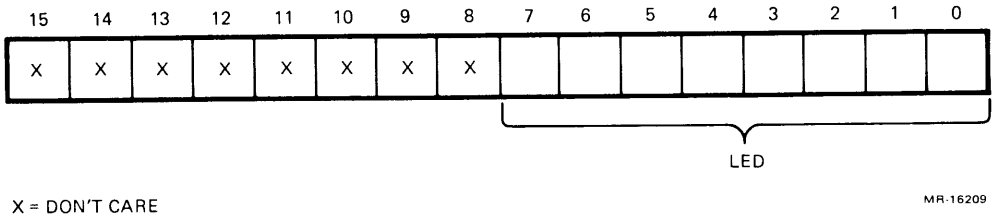

Figure 4-17 Boot and Diagnostic Configuration Register Format

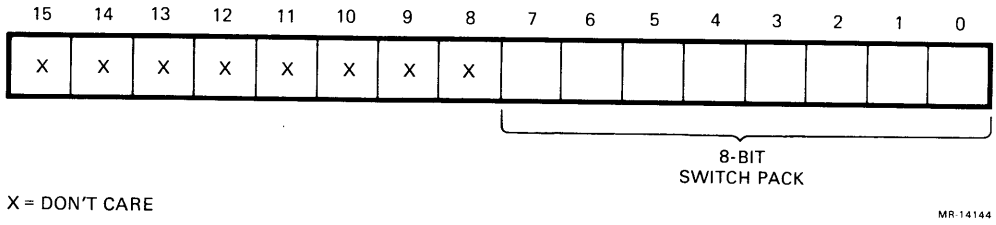

Figure 4-18 Display Register

Table 4-13 Display Register Bit Descriptions

Bit(s)	Name	Function
15::06	—	Unused
05::00	LED 5-0	These bits enable the boot and diagnostic programs to light the LEDs located at the top of the CPU module. Clearing any of these bits lights the corresponding LED.

4.15 MAINTENANCE REGISTER (Address 17 777 750)

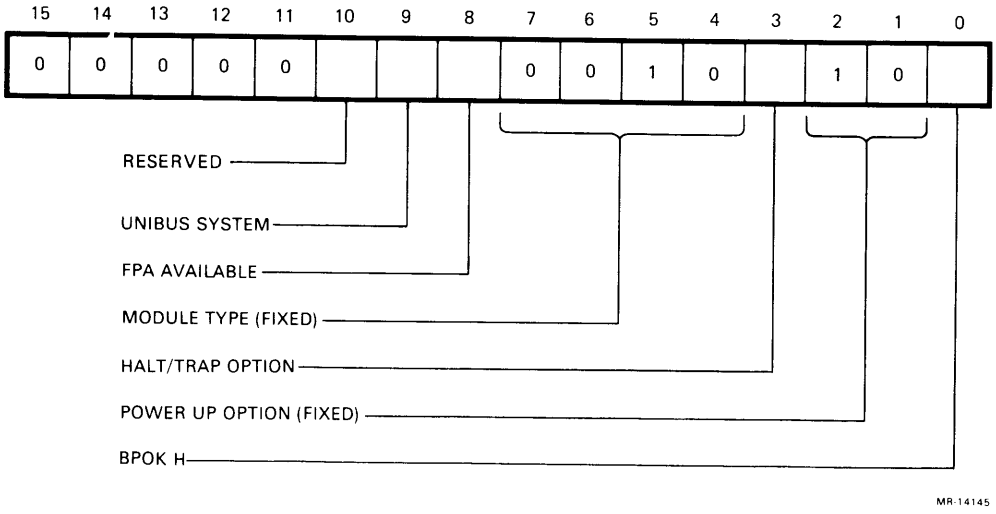

Figure 4-19 Maintenance Register Format

Table 4-14 Maintenance Register Bit Descriptions

Bit(s)	Name	Function
15:11	Unused.	Reserved for future expansion. Read as zeros.
10	—	Reserved for future use.
09	UNIBUS system (RO)	This bit reflects the status of the externally applied UNIBUS adapter line. A "1" indicates that the system includes a UNIBUS adapter.
08	FPA	When set, this bit indicates that the FPA is available for use. **NOTE** **This bit is not used with the KDJ11-BC CPU module.**
07:04	Module type	This 4-bit code is hard-wired as a "2", indicating a KDJ11-B module.
03	Halt/trap (R/W)	This read/write bit determines the response of a processor to a kernel mode halt instruction. Setting the bit selects the trap option, causing the CPU to trap to location 4. Clearing the bit selects the halt option, causing the CPU to halt and enter ODT. This bit is cleared by the negation of DCOK and is set by the boot and diagnostic ROM code if the trap option is selected by a bit in the configuration RAM. The trap option is not intended for normal use and is reserved for controller applications.
02-01	Power-up code	This 2-bit code is hard-wired as a "2". At power-up, the processor sets the PC to 173000 and sets the PSW to 370. It then starts program execution at location 173000, which is the starting location for the KDJ11-B boot and diagnostic ROM program. These programs test out the KDJ11-B module and then implement the user-selected power-up option specified in the configuration data.
00	BPOK H	This bit is set (1) if the PMI BUS signal BPOK H is asserted, indicating that ac power is okay.

4.16 BOOT AND DIAGNOSTIC CONTROLLER REGISTER (Address: 17 777 520)

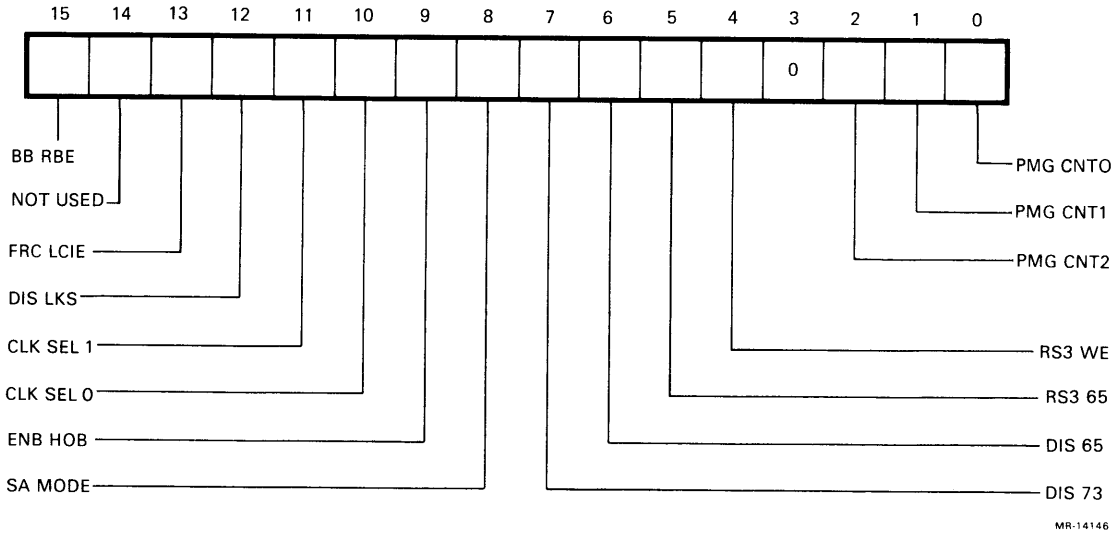

Figure 4-20 Boot and Diagnostic Controller Register Format

Table 4-15 Boot and Diagnostic Controller Register Bit Descriptions

Bit(s)	Name	Function
15	Not used	Reserved for future use.
14	Not used	Could be a "1" or "0".
13	Force line clock interrupt enable (FRC LCIE)	If this bit is set, assertion of the signal selected by BCSR <11,10> (clock select bits 1 and 0) will unconditionally request interrupts. If FRC LCIE is clear, assertion of the selected signal will request interrupts only if the line clock status register bit <6> (LCIE) is set under program control. FRC LCIE is cleared by the negation of DCOK.
12	Line clock status register disable (DIS LKS)	If this bit is set, the line clock status register (LKS) is disabled. If this bit is clear, LKS is enabled and responds to bus address 17777546. DIS LKS is cleared by the negation of DCOK.
11 10	CLK SEL1 CLK SEL0	Clock select bits 1 and 0. These two bits select the source of the line clock interrupt request:

CLK SEL1	CLK SEL0	Source of Interrupt
0	0	External LTC line
0	1	On-board 50 Hz
1	0	On-board 60 Hz
1	1	On-board 800 Hz

Table 4-15 Boot and Diagnostic Controller Register Bit Descriptions (Cont.)

Bit(s)	Name	Function
		Both bits are cleared by the negation of DCOK.
09	Enable halt on break (ENB HOB) (R/W)	When this bit is set, the console serial line unit halt on break feature is enabled. When this bit is clear, the feature is disabled. ENB HOB is cleared by the negation of DCOK.
08	Standalone mode (SA MODE) (R/W)	When this bit is set, the KDJ11-B operates in standalone mode, using its cache as main memory. External memory and peripherals are all disabled. When SA MODE is clear, standalone mode is turned off, enabling external memory and peripherals. SA MODE is set by the negation of DCOK.
07	Disable 17 773 000 (DIS 73) (R/W)	When this bit is set, response of the 16-bit ROM memory to addresses 17 773 000 - 17 773 776 is disabled, allowing the operation of an external ROM that uses those addresses. When DIS 73 is clear, the 16-bit ROMs respond to those addresses, using the high byte of the page control register as the most significant address bits. DIS 73 is cleared by the negation of DCOK.
06	Disable 17 765 000 (DIS 65) (R/W)	When this bit is set, response of the boot and diagnostic 16-bit and 8-bit ROM memory to addresses 17 765 000 - 17 765 776 is disabled, and allows the operation of external ROM which uses those addresses. When DIS 65 is clear, the ROM memory selected by BCSR <5> responds to those addresses, using the low byte of the page control register as the most significant address bits. DIS 65 is cleared by the negation of DCOK.
05	ROM socket 3 at 17 765 000 (RS3 65) (R/W)	This bit selects whether there is a 16-bit ROM in ROM sockets one and two, or there is an 8-bit ROM in ROM socket three, and responds to addresses 17 765 000 17 765 776 (assuming that BCSR <4> is clear). If RS3 65 is set, the 8-bit ROM is selected. If RS3 65 is clear, the 16-bit ROM is selected. In either case, the low byte of the page control register provides the most significant address bits. RS3 65 is cleared by the negation of DCOK.
04	ROM socket 3 write enable (RS3 WE)	If BCSR <6> (DIS 65) is clear, and if BCSR <5> and <4> (RS3 65 and RS3 WE) are both set, then the program can write access ROM socket 3 which typically contains an EEPROM. RS3 WE is cleared by power-up and by bus initialize.

Table 4-15 Boot and Diagnostic Controller Register Bit Descriptions (Cont.)

Bit(s)	Name	Function
03	Unused	This bit always reads as "0".
02 01 00	Processor mastership grant count bits 2, 1, and 0 (PMG CNT2) (PMG CNT1) (PMG CNT0)	These three bits enable the PMG counter and select the length of time for PMG counter overflow. When enabled, the PMG counter begins counting when the KDJ11-B must access an I/O page location or external memory. Counter overflow causes the KDJ11-B to suppress all DMA requests and give the processor bus mastership during the next DMA arbitration cycle. When the PMG counter is disabled, the processor is blocked from bus mastership as long as DMA requests are pending. All three bits are cleared by the negation of DCOK.

PMG CNT2	PMG CNT1	PMG CNT0	Count Time
0	0	0	(Disabled) *
0	0	1	0.4 μs
0	1	0	0.8 μs
0	1	1	1.6 μs
1	0	0	3.2 μs
1	0	1	6.4 μs
1	1	0	12.8 μs
1	1	1	25.6 μs

* The PMG count of 0 (disabled) is not recommended for most typical systems, and is reserved for special applications.

4.17 PAGE CONTROL REGISTER (Address 17 777 522)

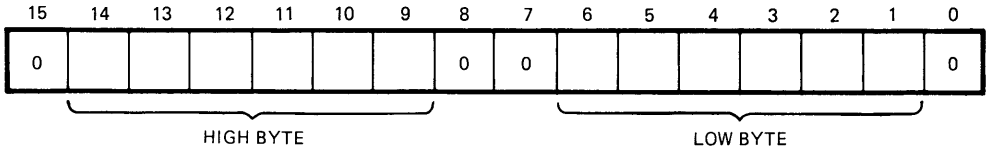

Figure 4-21 Page Control Register Format

Table 4-16 Page Control Register Bit Descriptions

Bit(s)	Name	Function
15	Not used	Always read as "0".
14:09	High byte (R/W)	These six bits provide the most significant ROM address bits when the 16-bit ROM sockets are accessed by bus addresses 17 773 000 – 17 773 776.
08:07	Not used	Always read as "0".
06:01	Low byte (R/W)	These six bits provide the most significant ROM (or EEPROM) address bits when the 16-bit or the 8-bit ROM (or EEPROM) sockets are accessed by bus addresses 17 765 000 – 17 765 776.
00	Not used	Always read as "0".

4.18 LINE FREQUENCY CLOCK STATUS REGISTER (Address 17 777 546)

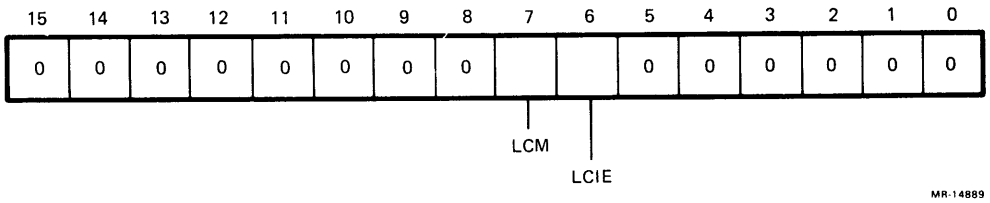

Figure 4-22 Clock Status Register Format

Table 4-17 Clock Status Register Bit Descriptions

Bit(s)	Name	Function
15:08	Unused	Always read as "0".
07	Line clock monitor (LCM) (R/W)	This bit is set by the leading edge of the external BEVENT line (or of one of the three on-board clock frequencies) and by bus initialize. LCM is cleared automatically on processor interrupts acknowledge. It is also cleared by writes to the LKS with bit <7> = "0".
06	Line clock interupt enable (LCIE) (R/W)	This bit, when set, causes the set condition of LCM (LKS <7>) to initiate a program interrupt request at a priority level of 6. When LCIE is clear, line clock interrupts are disabled. LCIE is cleared by power-up and by bus INIT. LCIE is held set INIT. LCIE is held set when BCSR <13> (FRC LCIE) is set.
05:00	Unused	Always read as "0".

4.19 RECEIVER STATUS REGISTER (Address 17 777 560)

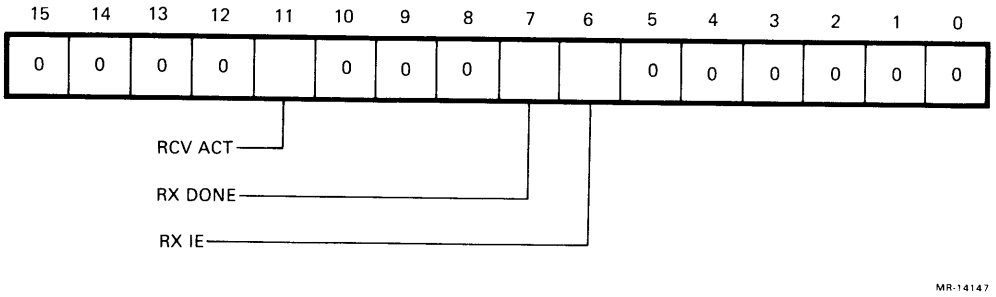

Figure 4-23 Receiver Status Register Format

Table 4-18 Receiver Status Register Bit Descriptions

Bit(s)	Name	Function
15:12	Unused	Read as "0".
11	Receiver active (RCV ACT) (RO)	This bit is set at the center of the start bit of the serial input data and is cleared at the expected center (per DLART timing) of the stop bit at the end of the serial data. Receiver done (RX DONE) is set one bit time after RCV ACT is cleared.
10:08	Unused	Read as "0".
07	Receiver done (RX DONE) (RO)	This bit is set when an entire character has been received and is ready to be read from the RBUF register. This bit is automatically cleared when RBUF is read. It is also cleared by power-up.
06	Receiver interupt enable (RX IE) (R/W)	This bit is cleared by power-up and bus INIT. If both RCVR DONE and RCVR INT ENB are set, a program interrupt is requested.
05:00	Unused	Read as "0".

4.20 RECEIVER DATA BUFFER (Address 17 777 562)

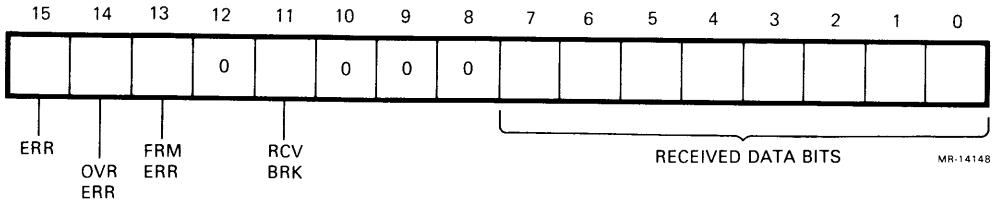

Figure 4-24 Received Data Buffer Register Format

Table 4-19 Received Data Buffer Register Bit Descriptions

Bit(s)	Name	Function
15	Error (ERR) (RO)	This bit is set if RBUF <14> or <13> is set. ERR is cleared if these two bits are cleared. This bit cannot generate a program interrupt.
14	Overrun error (OVR ERR) (RO)	This bit is set if a previously received character was not read before being overwritten by the present character.
13	Framing error (FRM ERR) (RO)	This bit is set if the present character had no valid stop bit. This bit is used to detect break.
		NOTE **Error conditions remain present until the next character is received, at which point the error bits are updated. The error bits are not necessarily cleared by power-up.**
12	Unused	This bit always reads as "0".
11	Received break (RCV BRK) (RO)	This bit is set at the end of a received character for the serial data input remained in the SPACE condition for all 11-bit time. RCV BRK then remains set until the serial data input returns to the MARK condition.
10:08	Unused	These bits always read as "0".
07:00	Received data bits	These read-only bits contain the last received character.

4.21 TRANSMITTER STATUS REGISTER (Address 17 777 564)

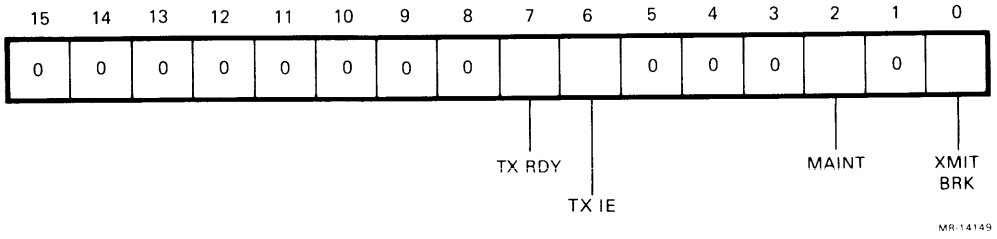

Figure 4-25 Transmit Status Register Format

Table 4-20 Transmit Status Register Bit Descriptions

Bit(s)	Name	Function
15:08	Unused	Read as "0".
07	Transmitter ready (TX RDY) (RO)	This bit is cleared when XBUF is loaded and sets when XBUF can receive another character. XMT RDY is set by power-up and by bus INIT.
06	Transmitter interrupt enable (TX IE) (R/W)	This bit is cleared by power-up and by bus INIT. If both TX RDY and TX IE are set, a program interrupt is requested.
05:03	Unused	Read as "0".
02	Maintenance (MAINT) (RO)	This bit is used to facilitate a maintenance self-test. When MAINT is set, the external serial input is disconnected and the serial output is used as the serial input. This bit is cleared by power-up and by bus INIT.
01	Unused	Read as "0".
00	Transmit break (XMIT BRK) (R/W)	When this bit is set, the serial output is forced to the SPACE condition. XMIT BRK is cleared by power-up and by bus INIT.

4.22 TRANSMITTER DATA BUFFER REGISTER (Address 17 777 566)

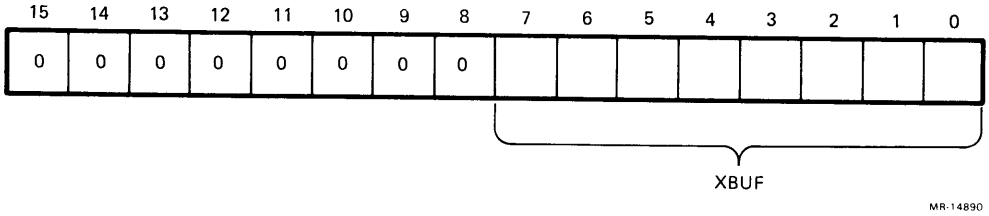

Figure 4-26 Transmitter Data Buffer Register Format

Table 4-21 Transmitter Data Buffer Register Bit Descriptions

Bit(s)	Name	Function
15:08	Unused	Always read as "0".
07:00	XBUF (WO)	These eight bits are used to load the transmited character.

4.23 UNIBUS MAPPING REGISTERS

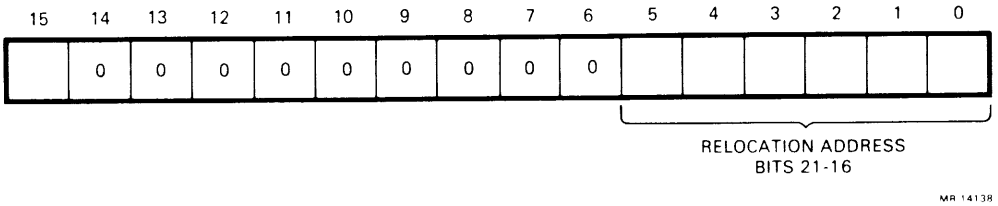

Figure 4-27 Hi-Address Register Format

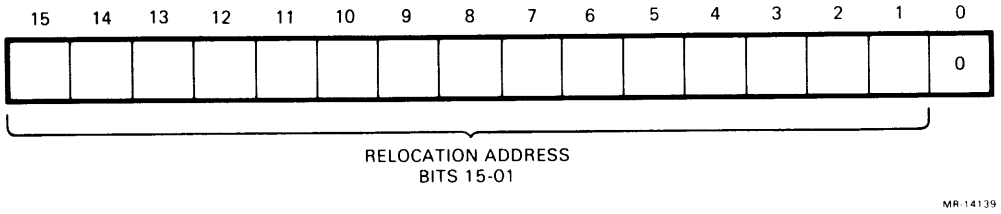

Figure 4-28 Lo-Address Register Format

Table 4-22 UNIBUS Map Register Pairs

Register Pair No.	I/O Page Addresses Lo-Register	Hi-Register	UNIBUS Addresses Mapped via Register Pair
0	17 770 200	17 770 202	000 000 - 017 777
1	17 770 204	17 770 206	020 000 - 037 777
2	17 770 210	17 770 212	040 000 - 057 777
3	17 770 214	17 770 216	060 000 - 077 777
4	17 770 220	17 770 222	100 000 - 117 777
5	17 770 224	17 770 226	120 000 - 137 777
6	17 770 230	17 770 232	140 000 - 157 777
7	17 770 234	17 770 236	160 000 - 177 777
10	17 770 240	17 770 242	200 000 - 217 777
11	17 770 244	17 770 246	220 000 - 237 777
12	17 770 250	17 770 252	240 000 - 257 777
13	17 770 254	17 770 256	260 000 - 277 777
14	17 770 260	17 770 262	300 000 - 317 777
15	17 770 264	17 770 266	320 000 - 337 777
16	17 770 270	17 770 272	340 000 - 357 777
17	17 770 274	17 770 276	360 000 - 377 777
20	17 770 300	17 770 302	400 000 - 417 777
21	17 770 304	17 770 306	420 000 - 437 777
22	17 770 310	17 770 312	440 000 - 457 777
23	17 770 314	17 770 316	460 000 - 477 777

Table 4-22 UNIBUS Map Register Pairs (Cont.)

Register Pair No.	I/O Page Addresses Lo-Register	Hi-Register	UNIBUS Addresses Mapped via Register Pair
24	17 770 320	17 770 322	500 000 - 517 777
25	17 770 324	17 770 326	520 000 - 537 777
26	17 770 330	17 770 332	540 000 - 557 777
27	17 770 334	17 770 336	560 000 - 577 777
30	17 770 340	17 770 342	600 000 - 617 777
31	17 770 344	17 770 346	620 000 - 637 777
32	17 770 350	17 770 352	640 000 - 657 777
33	17 770 354	17 770356	660 000 - 677 777
34	17 770 360	17 770 362	700 000 - 717 777
35	17 770 364	17 770 366	720 000 - 737 777
36	17 770 370	17 770 372	740 000 - 757 777
37 *	17 770 374	17 770 376	I/O Page (No Relocation)

* Can be read or written into, but not used for mapping.

4.24 OPTIONAL UNIBUS MEMORY

Table 4-23 lists the UNIBUS address space allocated by the various memory configuration register (KMCR) bit codes.

Table 4-23 Register Selection of UNIBUS Memory

KMCR Register Bits 04	03	02	01	00	UNIBUS Memory Size	UNIBUS Memory Address Range
0	0	0	0	0	0 Kbyte	
0	0	0	0	1	8 Kbyte	XX 740 000 - XX 757 777
0	0	0	1	1	16 Kbyte	XX 720 000 - XX 757 777
0	0	1	0	0	24 Kbyte	XX 700 000 - XX 757 777
0	0	1	0	1	32 Kbyte	XX 660 000 - XX 757 777
0	0	1	1	0	40 Kbyte	XX 640 000 - XX 757 777
0	0	1	1	1	48 Kbyte	XX 620 000 - XX 757 777
					56 Kbyte	XX 600 000 - XX 757 777
0	1	0	0	0	64 Kbyte	XX 560 000 - XX 757 777
0	1	0	0	1	72 Kbyte	XX 540 000 - XX 757 777
0	1	0	1	0	80 Kbyte	XX 520 000 - XX 757 777
0	1	0	1	1	88 Kbyte	XX 500 000 - XX 757 777
0	1	1	0	0	96 Kbyte	XX 460 000 - XX 757 777
0	1	1	0	1	104 Kbyte	XX 440 000 - XX 757 777
0	1	1	1	0	112 Kbyte	XX 420 000 - XX 757 777
0	1	1	1	1	120 Kbyte	XX 400 000 - XX 757 777

Table 4-23 Register Selection of UNIBUS Memory (Cont.)

KMCR Register Bits 04	03	02	01	00	UNIBUS Memory Size	UNIBUS Memory Address Range
1	0	0	0	0	128 Kbyte	XX 360 000 - XX 757 777
1	0	0	0	1	136 Kbyte	XX 340 000 - XX 757 777
1	0	0	1	0	144 Kbyte	XX 320 000 - XX 757 777
1	0	0	1	1	152 Kbyte	XX 300 000 - XX 757 777
1	0	1	0	0	160 Kbyte	XX 260 000 - XX 757 777
1	0	1	0	1	168 Kbyte	XX 240 000 - XX 757 777
1	0	1	1	0	176 Kbyte	XX 220 000 - XX 757 777
1	0	1	1	1	184 Kbyte	XX 220 000 - XX 757 777
1	1	0	0	0	192 Kbyte	XX 160 000 - XX 757 777
1	1	0	0	1	200 Kbyte	XX 140 000 - XX 757 777
1	1	0	1	0	208 Kbyte	XX 120 000 - XX 757 777
1	1	0	1	1	216 Kbyte	XX 100 000 - XX 757 777
1	1	1	0	0	224 Kbyte	XX 060 000 - XX 757 777
1	1	1	0	1	232 Kbyte	XX 040 000 - XX 757 777
1	1	1	1	0	240 Kbyte	XX 020 000 - XX 757 777
1	1	1	1	1	248 Kbyte	XX 000 000 - XX 757 777

NOTE
XX = 17 for KMCR <05> = "0" (22-bit mode).
XX = 00 for KMCR <05> = "1" (18-bit mode).

4.25 MEMORY CONFIGURATION REGISTER (KMCR - Address 17 777 734)

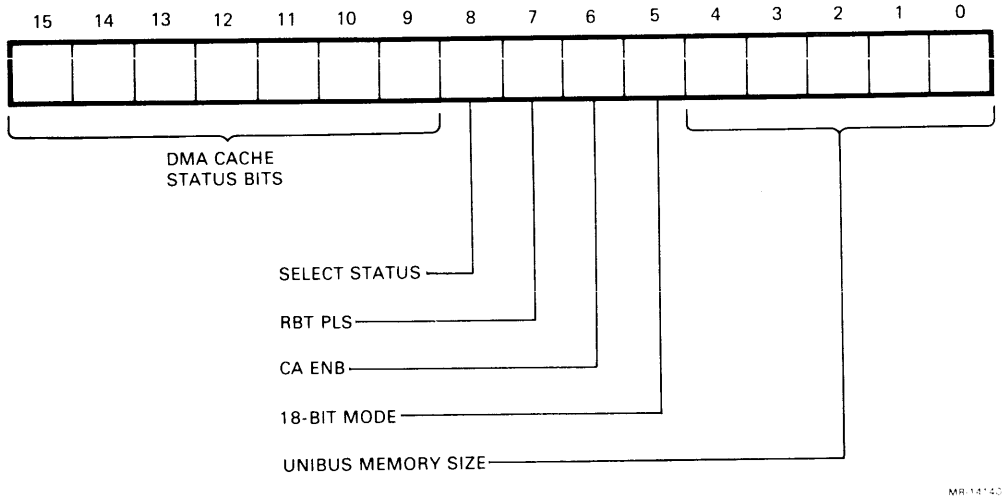

Figure 4-29 Memory Configuration Register

Table 4-24 Memory Configuration Register Bit Descriptions

Bit(s)	Name	Function
15:09	DMA cache status bits (RO)	These seven bits reflect the status of the DMA cache. KMCR <15> is DMA cache hit. The content of KMCR <14:09> depends upon the value of the value of the KMCR <08> (status select).
08	Status select (R/W)	This bit selects the content of KMCR <15-09> (Tables 4-25 and 4-26).
07	Reboot pulse (RBT PLS) (RO)	This bit is set by the front panel reboot pulse which also generates a KTJ11-B power-down/power-up cycle. RBT PLS is not cleared by the assertion of DC LO during the KTJ11-B power-down/power-up cycle initiated by the front panel reboot pulse, but it is cleared by any other DC LO assertion.
06	Cache enable (CA ENB) (R/W)	This bit, when set, enables the DMA cache. When CA ENB is clear, the DMA cache is disabled. CA ENB is cleared by the assertion of DC LO.
05	18-Bit mode (R/W)	When this bit is set, the CPU can access UNIBUS memory only when address bits <21:18> = 00. When this bit is clear, they can access UNIBUS memory if address bits <21:18> = 17. This bit is cleared by the assertion of DC LO. Write access to this bit is disabled when diagnostic controller status register (DCSR) <08> (diagnostic mode) is clear.
04:00	UNIBUS memory size	If the system contains main memory only (no UNIBUS memory), these five bits, as well as KMCR <05>, must be cleared. If the system contains UNIBUS memory only (no main memory), then KMCR <05:00> must be set. If the system contains both main memory and UNIBUS memory, KMCR <04:00> indicate the number of 8 Kbyte address segments assigned to UNIBUS memory. As described in section 3.4, UNIBUS memory is assigned downward, starting with the segment below the I/O page. These bits are cleared by assertion of DC LO. Write access to these bits is disabled when DCSR <08> (diagnostic mode) is clear.

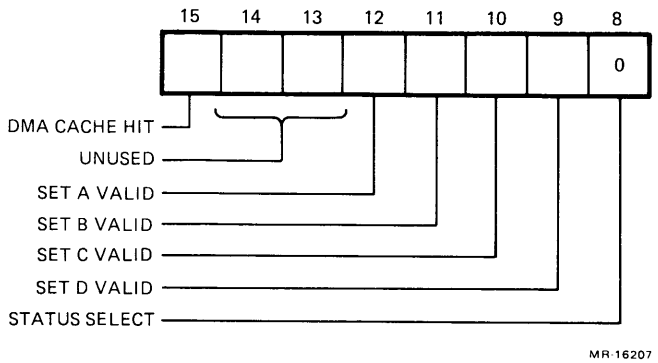

Figure 4-30 Status Select = 0 Field Format

Table 4-25 Status Select = 0 Field Description

Bit(s)	Name	Function
15	DMA cache hit	This bit is updated during all writes to main memory, and all reads from main memory. It is set if a cache hit is detected, and cleared if a cache miss is detected. This bit is cleared when KMCR <6> is clear.
14-13	Unused	Always read as "0".
12	Set A valid	Reflects the current status of the valid bit corresponding to set A. The bit is cleared when KMCR <6> is clear.
11	Set B valid	Reflects the current status of the valid bit corresponding to set B. The bit is cleared when KMCR <6> is clear.
10	Set C valid	Reflects the current status of the valid bit corresponding to set C. The bit is cleared when KMCR <6> is clear.
09	Set D valid	Reflects the current status of the valid bit corresponding to set D. The bit is cleared when KMCR <6> is clear.

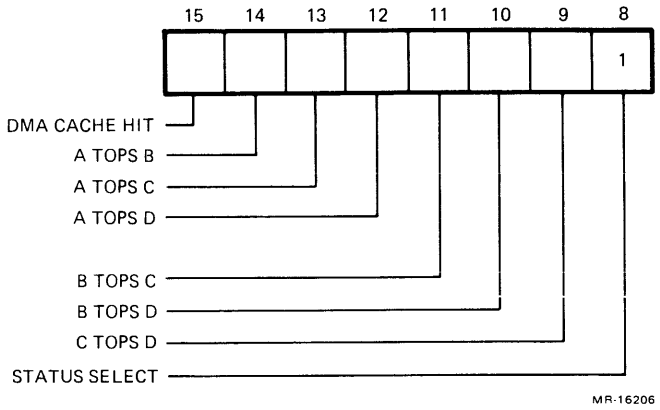

Figure 4-31 Select Status = 1 Field Format

Table 4-26 Select Status = 1 Field Description

Bit(s)	Name	Function
15	DMA cache hit	This bit is updated during all writes to main memory, and all DMA reads from main memory. It is set if a cache hit is detected, and cleared if a cache miss is detected. The bit is cleared when KMCR <6> is clear.
14	A Tops B (ATPSB)	If ATPSB is set, set A is more available than set B. If ATPSB is clear, set B is more available than set A. ATPSB is set when KMCR <6> is clear, when set A becomes the next available set, and when set B becomes the least available set. ATPSB is cleared when set B becomes the next available set, and when set A becomes the least available set.
13	A Tops C (ATPSC)	If ATPSC is set, set A is more available than set C. If ATPSC is clear, set C is more available than set A. ATPSC is set when KMCR <6> is clear, when set A becomes the next available set, and when set C becomes the least available set. ATPSC is cleared when set C becomes the next available set, and when set A becomes the least available set.
12	A Tops D (ATPSD)	If ATPSD is set, set A is more available than set D. If ATPSD is clear, set D is more available than set A. ATPSD is set when KMCR <6> is clear, when set A becomes the next available set, and when set D becomes the least available set. ATPSD is cleared when set D becomes the next available set, and when set A becomes the least available set.
11	B Tops C (BTPSC)	If BTPSC is set, set B is more available than set C. If BTPSC is clear, set C is more available than set B. BTPSC is set when KMCR <6> is clear, when set B becomes the next available set, and when set C becomes the least available set. BTPSC is cleared when set C becomes the next available set, and when set B becomes the least available set.
10	B Tops D (BTPSD)	If BTPSD is set, set B is more available than set D. If BTPSD is clear, set D is more available than set B. BTPSD is set when KMCR <6> is clear, when set B becomes the next available set, and when set D becomes the least available set. BTPSD is cleared when set D becomes the next available set, and when set B becomes the least available set.
09	C Tops D (CTPSD)	If CTPSD is set, set C is more available than set D. If CTPSD is clear, set D is more available than set C. CTPSD is set when KMCR <6> is clear, when set C becomes the next available set, and when set D becomes the least available set. CTPSD is cleared when set D becomes the next available set, and when set C becomes the least available set.

4.26 DIAGNOSTIC CONTROLLER STATUS REGISTER (Address 17 777 730)

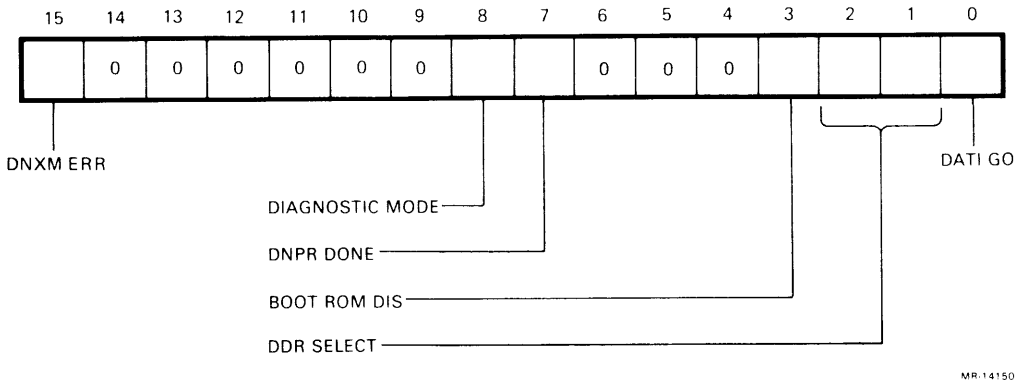

Figure 4-32 Diagnostic Controller Status Register Format

Table 4-27 Diagnostic Controller Status Register Bit Descriptions

Bit(s)	Name	Function
15	Diagnostic nonexistent memory error register (DNXM ERR)	This bit is cleared at the start of a diagnostic NPR cycle, and set if there is a nonexistent memory timeout during that cycle. DNXM ERR is also cleared when DCSR <08> (diagnostic mode) is cleared.
14:09	Unused	These bits always read as "0".
08	Diagnostic mode (R/W)	When this bit is set, the UNIBUS is disabled and the KTJ11-B is configured for diagnostic mode. When this bit is clear, the UNIBUS is enabled and the KTJ11-B is configured for normal operation. This bit is set by the assertion of DC LO.
07	DNPR done	This bit is set when there are no diagnostic NPR cycles pending. DNPR done is cleared by a write to DCSR with a "1" in bit 00, and by any write to the diagnostic data register (DDR). DNPR done is set by bus INIT or by completion of a diagnostic NPR cycle.
06:04	Unused	These bits always read as "0".
03	Boot ROM disable (R/W)	When this bit is set, response of the UBA boot ROM at addresses 177 773 000 - 177 773 776 is disabled, allowing operation of any external ROM which uses those addresses on the UNIBUS. When this bit is cleared, the UBA boot ROM responds to those addresses. This bit is cleared by the assertion of DC LO.
02:01	DDR select (R/W)	These two bits select the contents of the DDR during read operations. The DDR select bits are cleared by bus INIT.
00	DATI GO (WO)	Writing a "1" into this bit sets up a diagnostic data-in NPR cycle and clears DCSR bit 07. The NPR cycle is actually initiated by the next CPU read cycle which accesses the PMI. That cycle provides the address used in the NPR cycle. The data fetched during that cycle is loaded into the DDR.

4.27 DIAGNOSTIC DATA REGISTER (Address 17 777 732)

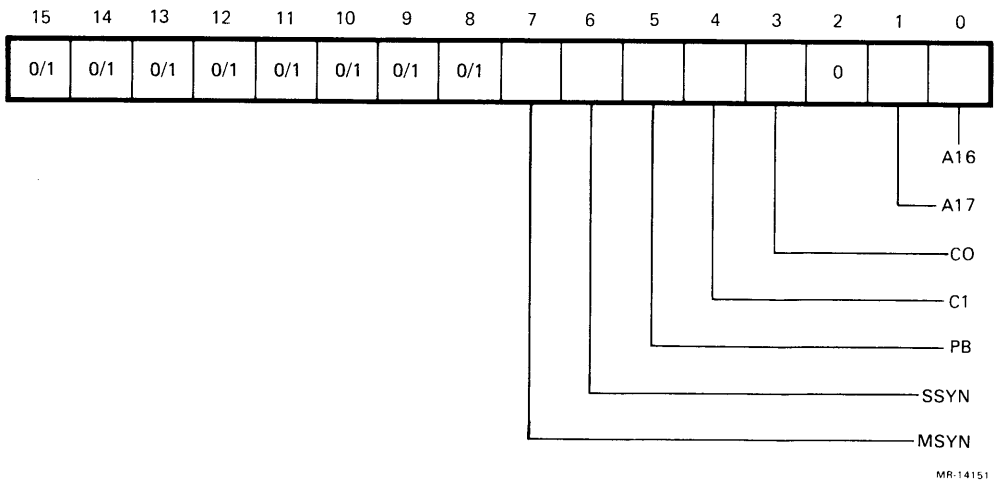

Figure 4-33 Diagnostic Data Register Format

Table 4-28 Diagnostic Data Register Content Descriptions

DDR Select Bits Bit 02	Bit 01	Content of Diagnostic Data Register
0	0	Diagnostic NPR register
0	1	UNIBUS data lines D15-00
1	0	UNIBUS address lines A15-00 *
1	1	UNIBUS address lines A17-16 and various UNIBUS control lines

* Asserted address line A16, during the diagnostic UNIBUS address lines read operation, may cause a parity error abort.

CHAPTER 5
OPTION INSTALLATION PROCEDURES

5.1 EXPANSION POWER SUPPLY INSTALLATION

The H7202-KB expansion power supply is installed for both types of expansion backplanes (i.e., DD11-CK and -DK) on P-series systems. Note that this power supply is standard on all A-series systems.

To install the expansion power supply on P-series systems, perform the following steps.

CAUTION

Remove the ac power cord from the outlet before performing Step 1.

1. Open the front door using the hex key.
2. Remove the card cage cover by pulling out the two plastic retainers.
3. Loosen the captive screws that secure the blower to the card cage.
4. Slide the blower assembly out approximately 6 inches. Disconnect the blower power plug.
5. Remove the blower from the cabinet by sliding it out and up.
6. Push in the tray lock (Figure 5-1). This releases the tray locking mechanism allowing it to be pulled forward for servicing.

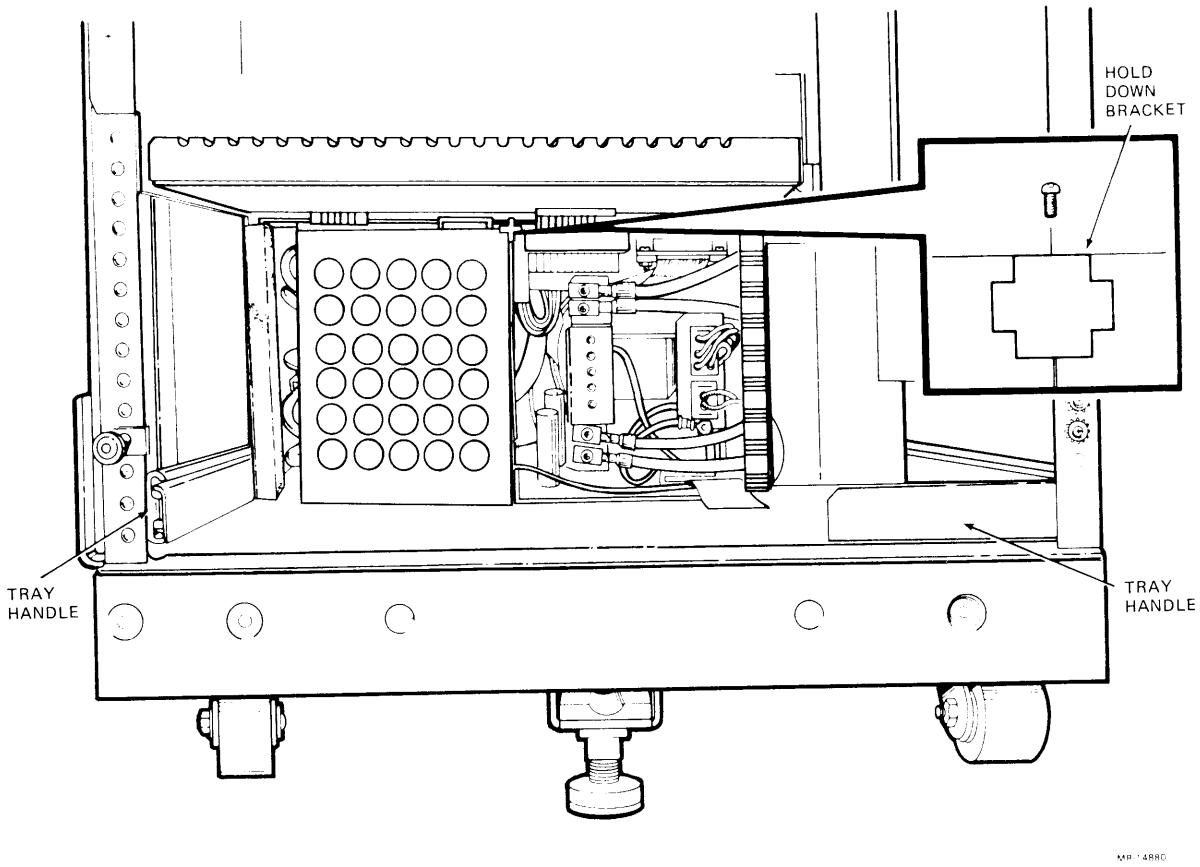

Figure 5-1 Expansion Power Supply Installation

7. Slide the tray forward by pulling on the tray handle until the second lock engages.
8. Loosen and remove the screw attached to the power supply hold-down bracket.
9. Remove and discard the baffle.
10. Place the power supply on the extended tray; insert the closed end of the supply first.
11. Once positioned inside the cabinet, guide the notched back of the supply into the slot.
12. After securing the back of the supply in the slot, replace the hold-down bracket securing the front end of both power supplies.
13. Plug in the two keyed cable connectors to the proper connector on the front of the expansion power supply.
14. Secure the cable bus wires to the bus bar located on the front of the expansion supply. Use a straight-slot screwdriver to secure both red bus wires to the bus bar end marked +5 V. Secure the two black cables to the bus bar end marked RTN.

15. Attach a ground wire from the cabinet frame to the front of the expansion supply.

16. Plug in the power connector to the proper connector on the front of the expansion supply.

17. Repeat steps 1 through 4 in reverse order.

5.2 EXPANSION BACKPLANE INSTALLATION

As shown in Figure 5-2, the two types of expansion backplanes are:

1. DD11-CK = 4-slot backplane

2. DD11-DK = 9-slot backplane

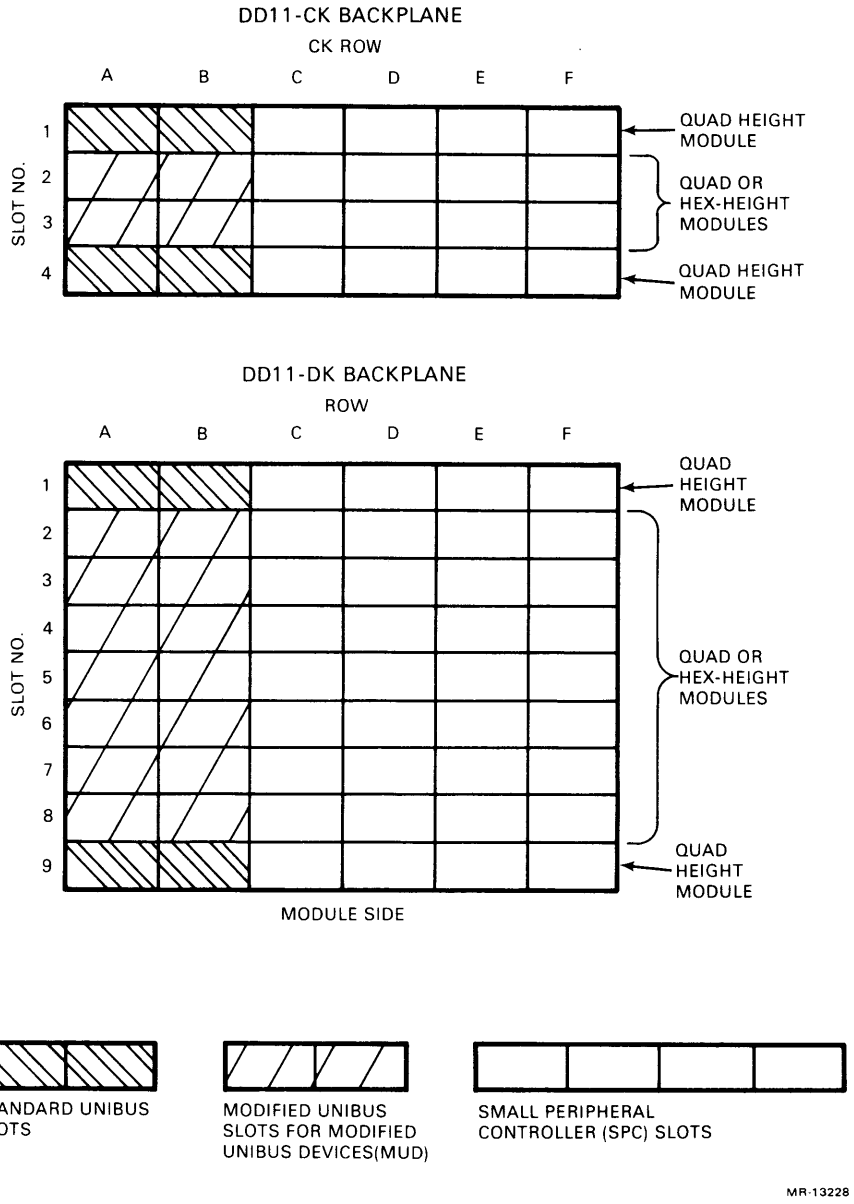

Figure 5-2 Expansion Backplane Slot Assignments

The standard UNIBUS connectors contain all the UNIBUS connections. Rows A and B of slot 1 are the beginning of the DD1-CK and -DK, and should be occupied by the BC11-A UNIBUS in-cable.

Rows A and B of slot 9 of the DD11-DK, or of slot 4 of the DD11-CK, are the end of the UNIBUS on the backplane. These slots should be occupied by the BC11-A UNIBUS out-cable or a terminator module (M9302 or M9312).

5.2.1 Backplane Installation Procedure

To install the expansion backplane assembly, perform the following steps.

1. Remove the ac power from the power controller by setting the circuit breaker to OFF (0).
2. Remove the back cover using a 4 mm (5/32-inch) hex wrench to release the door fasteners.
3. Lower the bulkhead panel after unscrewing the 10 screws.
4. Remove the left cabinet side cover (viewed from the cabinet front) by lifting up from the bottom (Figure 5-3).

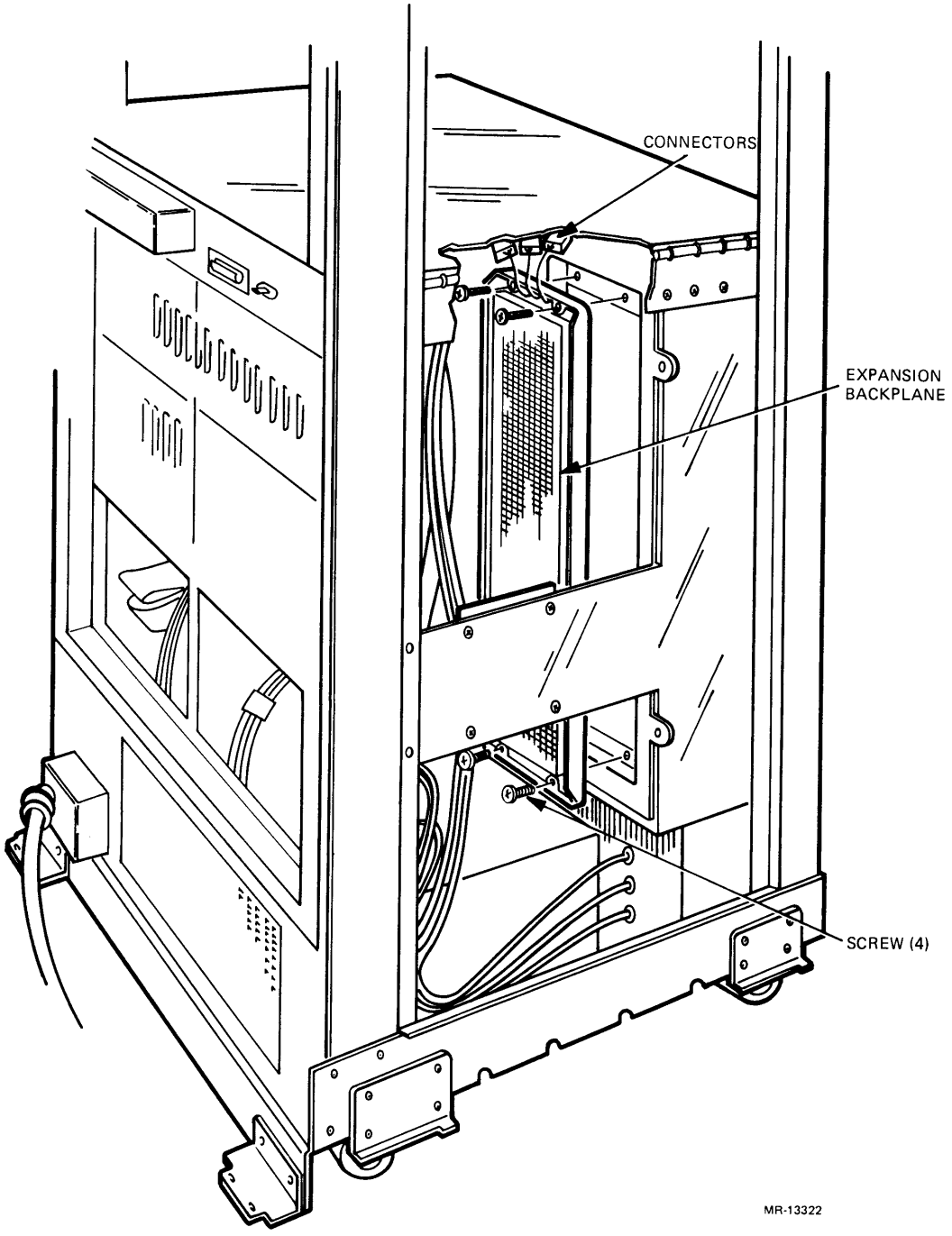

Figure 5-3 Expansion Backplane Mounting

5. Remove the side panel by unscrewing the four shoulder screws and two Phillips-head screws.

6. Remove the lexan (plastic) cover over the backplane and the metal insert(s) behind. Discard the metal insert; it is not reinstalled.

7. Position the expansion backplane through the front and align the two tapped screw holes for the DD11-CK, or the four tapped screw holes for the DD11-DK.

NOTE

The backplane harness includes a ground lead with a lug attached. The ground must be installed under the mounting screw.

If there are a sufficient number of NPG jumper modules, install the modules after removing NPG jumpers from backplane pins CA1 – CB1 for all slots.

8. Install the two/four 8-32 screws that are supplied with the backplane. Do not tighten the screws.

9. Install the backplane wiring harness connectors into the cabinet power distribution connectors.

10. Install two hex modules in each end slot of the backplane to align the slots.

11. Tighten the 8-32 screws installed in step 8.

12. Remove the hex modules from the backplane.

13. Replace the lexan cover on the backplane.

14. Replace the side panel using the four shoulder bolts and two Phillips-head screws.

15. Replace the outer side panel by aligning the two brackets above the shoulder bolts. Lower the cover brackets onto the shoulder bolts.

16. Close the rear panel bulkhead and tighten the captive mounting screws.

17. Close the front door and lock it with the hex key.

This completes the installation of a DD11-CK or DD11-DK optional backplane.

5.2.2 NPG and BG Jumper Lead Routing

The NPG line is the UNIBUS grant line for devices performing data transfers without processor intervention. Continuity of the NPG line is provided by wirewraps or jumpers on the backplane.

When an NPR device is placed in a slot, the corresponding jumper wire from pin CA1 to pin CB1 of that slot must be removed. The routing of the NPG signal through the backplane is shown in Figure 5-4. Grant priority decreases from slot 1 to slot 9 in the DD11-DK (slot 1 has highest priority and slot 9 has lowest).

NOTE

If an NPR device is removed from a slot, the jumper wire from CA1 to CB1 must be reconnected.

The bus grant lines (BG4 through BG7) for non-NPR devices are routed through each slot in row D. Grant priority for each level decreases from slot 1 to slot 9.

NOTE

A bus grant jumper card G727 in row D, or G7273 in row C and D must be installed in all unoccupied SPC slots. If an SPC slot is left open, bus grant continuity will be lost and the system will not operate.

NOTE

NPG routing wire wraps are for expansion backplanes only. CPU backplane has NPG routing DIP switch on the MDM.

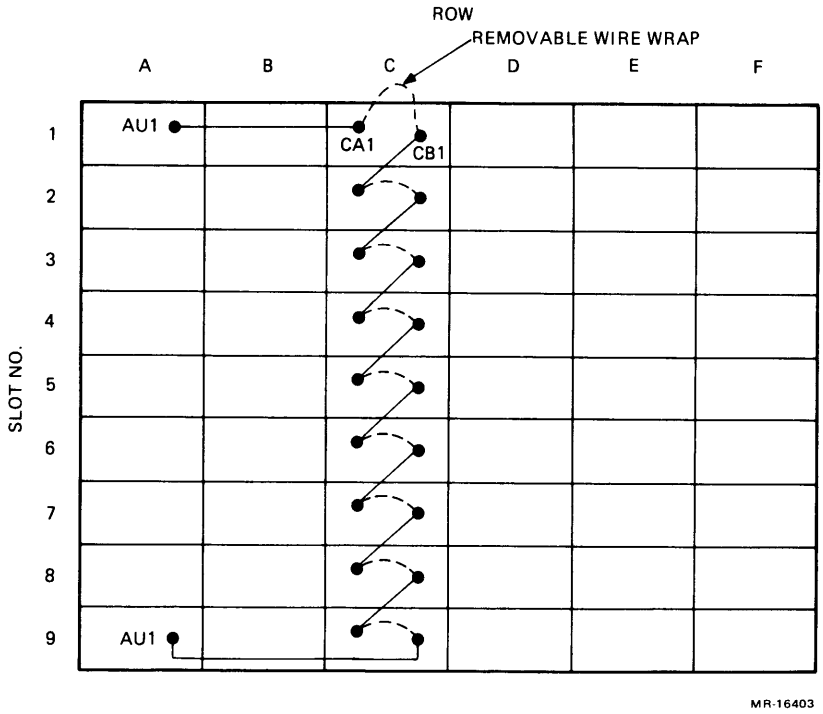

Figure 5-4 NPG Jumper Leads Routing

5.2.3 Backplane Power Connections

Power is supplied to the expansion backplane via a wire harness that connects the power distribution board with the power supply. The power wires run from the backplane to a set of Mate-N-Lok connectors wired directly into the distribution board.

The power harness from the DD11-DK contains two large connectors (15-pin Mate-N-Lok) and one small connector (6-pin Mate-N-Lok). The DD11-CK backplane has only one 15-pin connector and one 6-pin connector. The connector pin locations are shown in Figure 5-5 and the signal assignments for each pin are listed in Table 5-1 (DD11-CK) and Table 5-2 (DD11-dK).

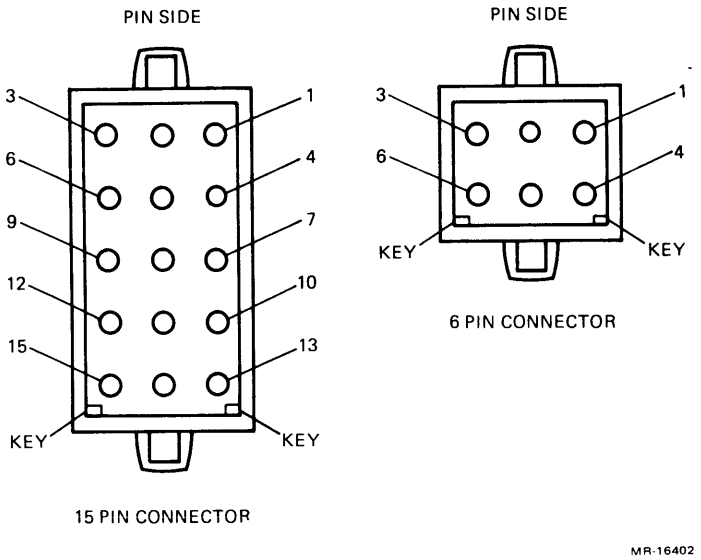

Figure 5-5 Backplane Connector Designations

Table 5-1 DD11-CK Power Connector Signal Assignments

Pin	Signal	Wire Gauge	Color
	15-Pin Mate-N-Lok Connector		
1	+5 V	14	Red
2	+15 V	18	Gray
3	Spare	–	Orange
4	+5 V	14	Red
5	Spare (not connected)	–	–
6	+15 V	18	Green
7	Ground	14	Black
8	Ground	14	Black
9	Spare (not connected)	–	–
10	Spare (not connected)	–	–
11	Spare (not connected)	–	–
12	+5 V	14	Red
13	-15 V	18	Blue
14	Spare	–	Brown
15	-15V	18	White
	6-Pin Mate-N-Lok Connector		
1	GND	18	Black
2	LTC (line clock)	18	Brown
3	DC LO	18	Violet
4	AC LO	18	Yellow
5	Spare (not connected)	–	–
6	Spare (not connected)	–	–

Table 5-2 DD11-DK Power Connector Signal Assignments

Pin	Signal	Wire Gauge	Color
	15-Pin Mate-N-Lok Connector 1		
1	+15 V	14	Red
2	+15 V	18	Gray
3	Spare	–	Orange
4	+5 V	14	Red
5	Spare (not connected)	–	–
6	Spare (not connected)	–	–
7	Spare (not connected)	–	–
8	Ground	14	Black
9	Ground	14	Black
10	Ground	14	Black
11	Spare (not connected)	–	–
12	+5 V	14	Red
13	Spare (not connected)	–	–
14	-5 V	18	Brown
15	Spare (not connected)	–	–

Table 5-2 DD11-DK Power Connector Signal Assignments (Cont.)

Pin	Signal	Wire Gauge	Color
	15-Pin Mate-N-Lok Connector 2		
1	+5 V	14	Red
2	Spare (not connected)	–	–
3	Spare	–	Orange
4	+5 V	14	Red
5	Spare (not connected)	–	–
6	+15 V	18	White
7	Spare (not connected)	–	–
8	Ground	14	Black
9	Ground	14	Black
10	Ground	14	Black
11	Spare (not connected)	–	–
12	Spare (not connected)	–	–
13	-15 V	18	Blue
14	Spare (not connected)	–	–
15	-15 V	18	Green
	6-Pin Mate-N-Lok Connector		
1	GND	18	Black
2	LTC (line clock)	18	Brown
3	DC LO	18	Violet
4	AC LO	18	Yellow
5	Spare (not connected)	–	–
6	Spare (not connected)	–	–

5.2.4 SPC Backplane Locations

The small peripheral control sections (C, D, E, and F) collectively contain all the UNIBUS lines as well as power voltages (+5 V, +15 V and -15 V). These sections can be used by hex height or quad height modules containing the control logic for peripheral devices. Appendix A shows the pin designations for the SPC backplane connectors.

Appendix A also shows the pin designations of the standard and modified UNIBUS connectors. The modified UNIBUS differs from the standard UNIBUS in that certain pins have been redesignated.

5.3 SPC MODULE INSTALLATION

CPU backplane slots 5 through 12 support the installation of UNIBUS SPC modules. Backplane slots 5 through 11 support both hex and quad SPC modules; slot 12 supports quad SPC modules only. Row A of slot 12 supports the UNIBUS out cable connector.

Hex height SPC modules occupy all four rows of the backplane while quad height occupy rows C through F. Quad height SPC modules, when installed, occupy the same backplane rows as the system CPU and memory modules.

To install an SPC module, perform the following steps.

1. Grasp the module by the two handles mounted at the top.

2. Install the module in the backplane slot by sliding it in along the card cage guides.

3. When the module is about three-quarters installed, grasp the handles (toward the module center) and swing them upwards, away from the module (Figure 5-6).

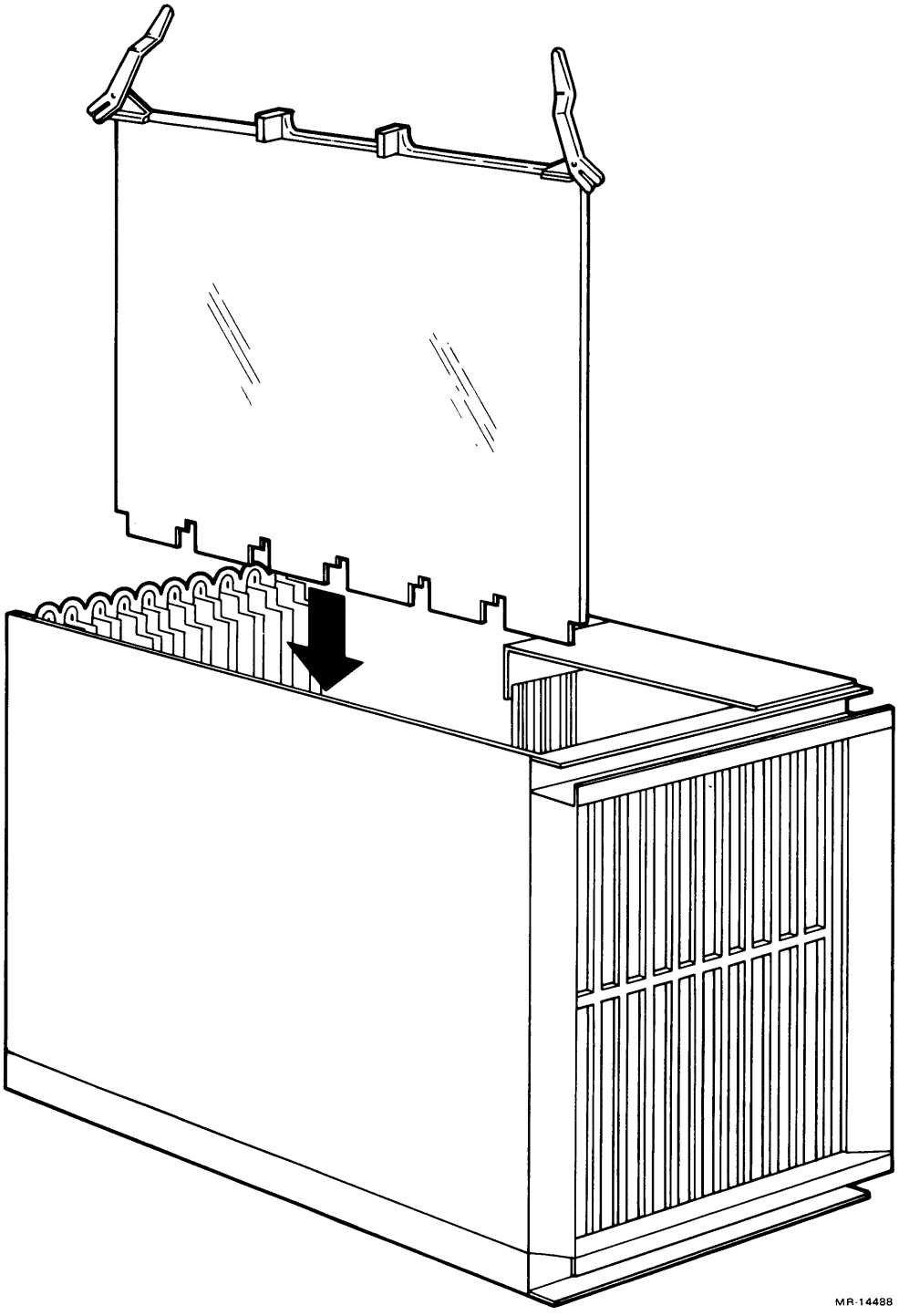

Figure 5-6 SPC Module Installation

4. Continue to slide the module into the backplane and press the handles downward. This action seats the module into the backplane connectors and secures the module handles' lower lip under the card cage frame.

This completes the installation procedure for an SPC module.

5.3.1 Cabinet SPC Cable Routing

Use the following directions for proper cable routing.

1. After installing an SPC in the appropriate backplane slot, the SPC cables are plugged into the connector and the cable is routed to the bulkhead assembly.

2. All SPC cables that plug into connectors mounted on the front edge of the module are routed toward the right side of the card cage as shown in Figure 5-7.

3. When the connector is mounted on the top of the module, the cable is routed up and over the cable hanger assembly located above the card cage.

4. If the connector is mounted near the module handle the installed cable is routed around the front of the card cage.

5. Located on the right side of the card cage are plastic cable clamps used to secure the SPC cable to the card cage. A bar is mounted horizontally behind the card cage and used to hang the SPC cables that are routed to the bulkhead.

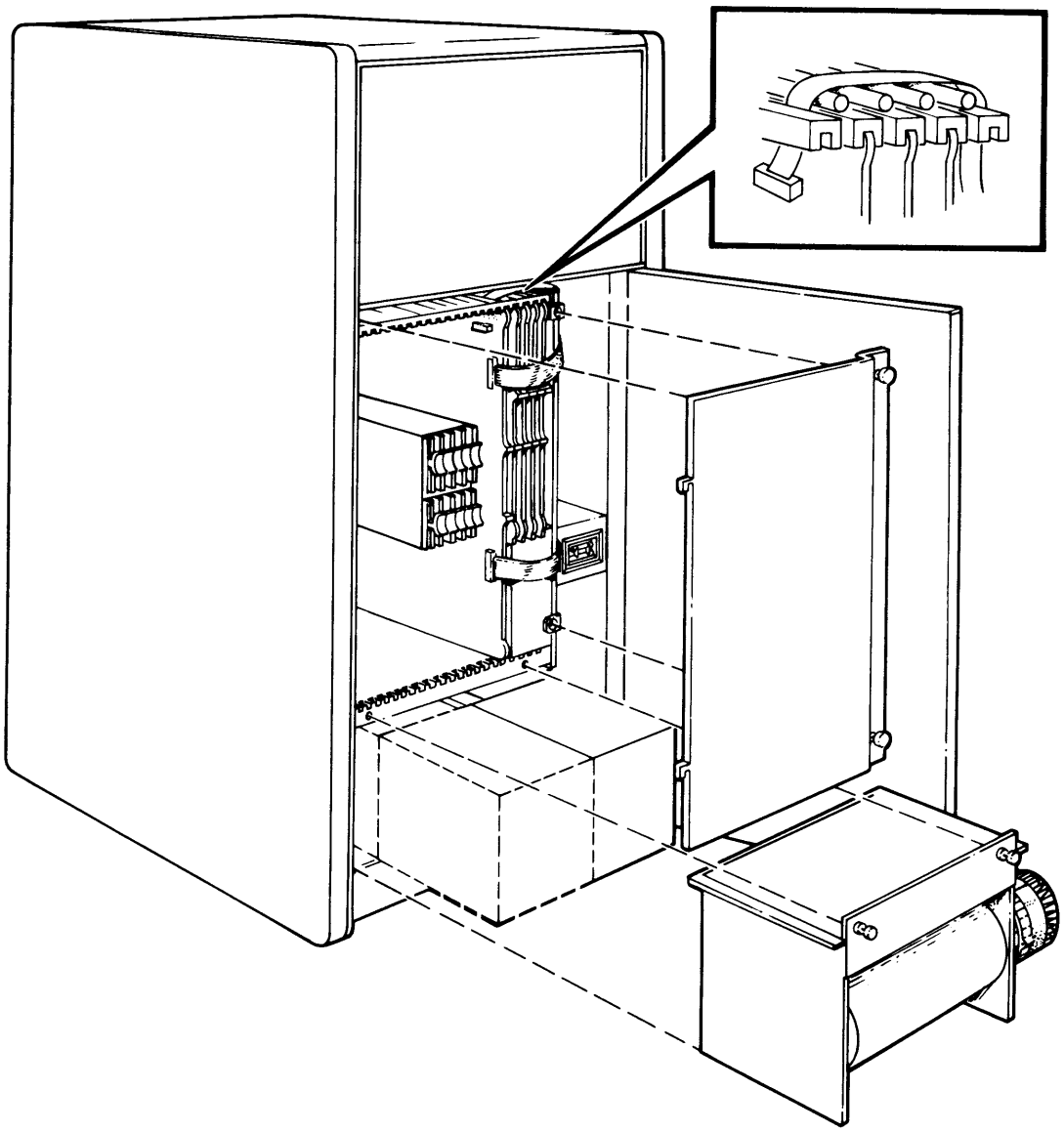

Figure 5-7 Cabinet SPC Cable Routing

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5.3.2 Box SPC Cable Routing

Use the following directions for proper cable routing.

1. After installing an SPC in the appropriate backplane slot, the SPC cables are plugged into the connector and the cable is routed to the bulkhead assembly.

2. The back panel has two bulkhead assembly areas, bottom left and top right (referenced from the rear).

3. Cables that plug into connectors mounted on the handle of the module are routed toward the lower left bulkhead.

4. Cables that plug into connectors mounted at the module top (installed in backplane) are routed to the upper right bulkhead (Figure 5-8).

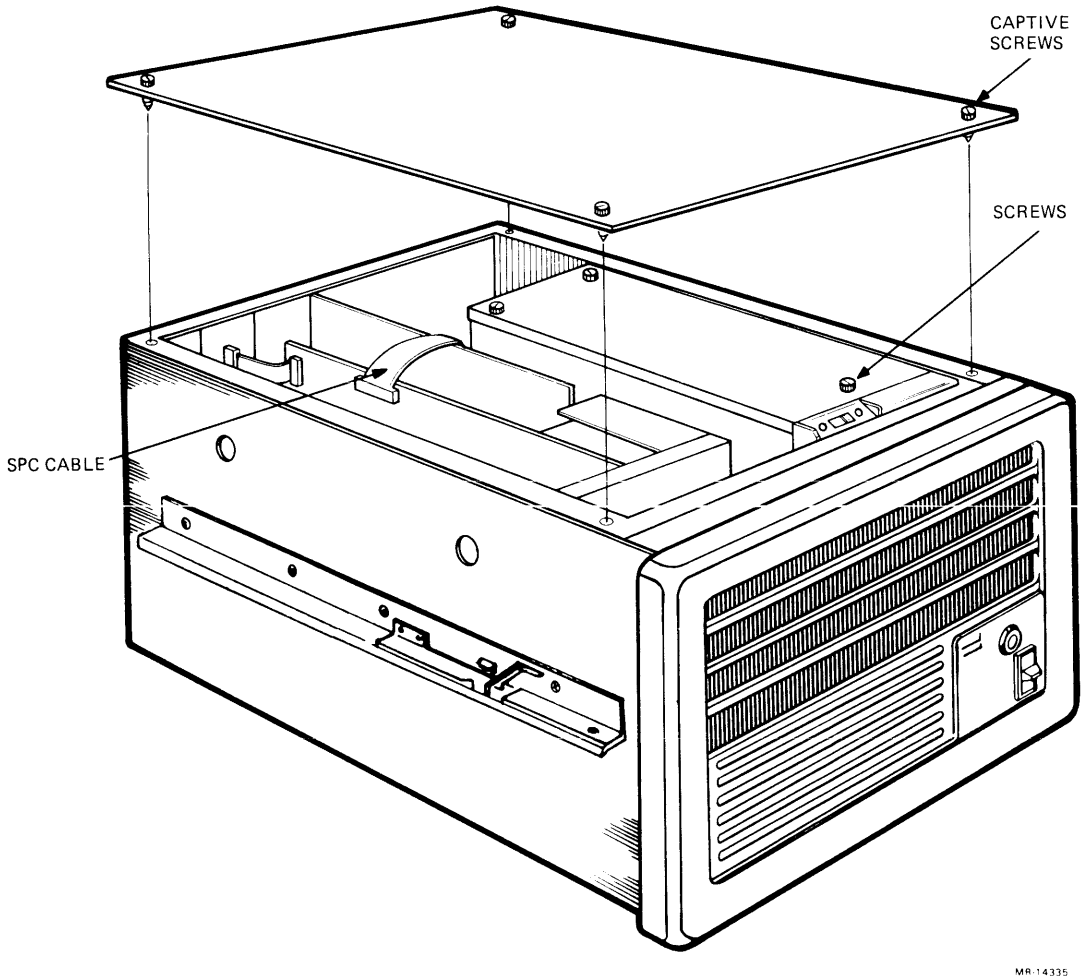

Figure 5-8 Box SPC Cable Routing

5.4 CABINET BATTERY BACK UP UNIT INSTALLATION

To install the BBU complete the following procedure.

CAUTION
The weight of the BBU is 19 kg (42 lbs); lifting and positioning of the BBU requires two people.

1. Unpack the BBU and installation kit.
2. Remove the BBU from the shipping container and place it on a flat surface.
3. Set the front panel TOY switch to OFF (Figure 5-9).

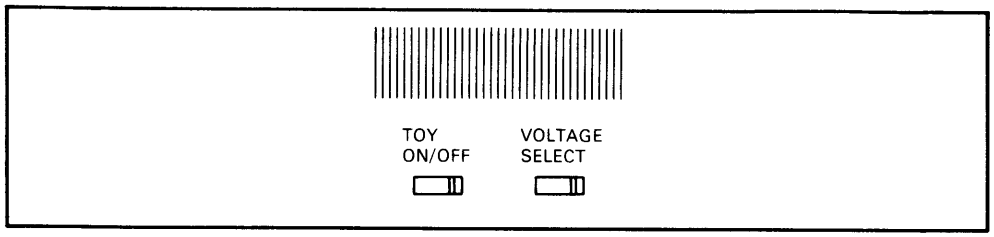

Figure 5-9 BBU Front Panel

4. Set the BBU VOLTAGE SELECT switch to match the site line voltage.
5. Set the rear BBU AC VOLTAGE SELECT to match the front panel VOLTAGE SELECT switch setting (Figure 5-10).

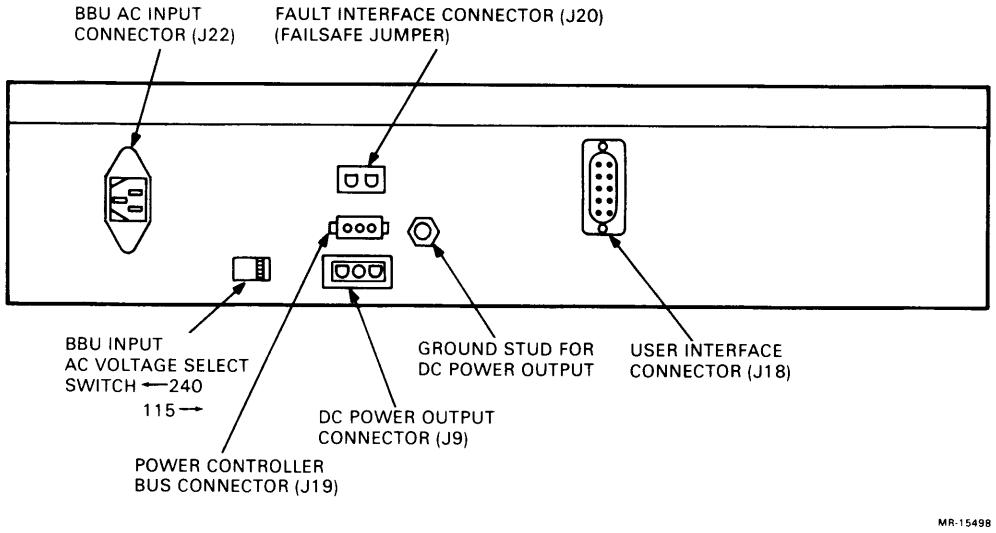

Figure 5-10 BBU Rear Panel

6. Open the front and rear cabinet doors using the hex key.
7. Turn off the power supply and power controller circuit breakers.
8. Unplug the ac power cord from the outlet.
9. Remove the cabinet right side panel by lifting it straight up from both sides (Figure 5-11).

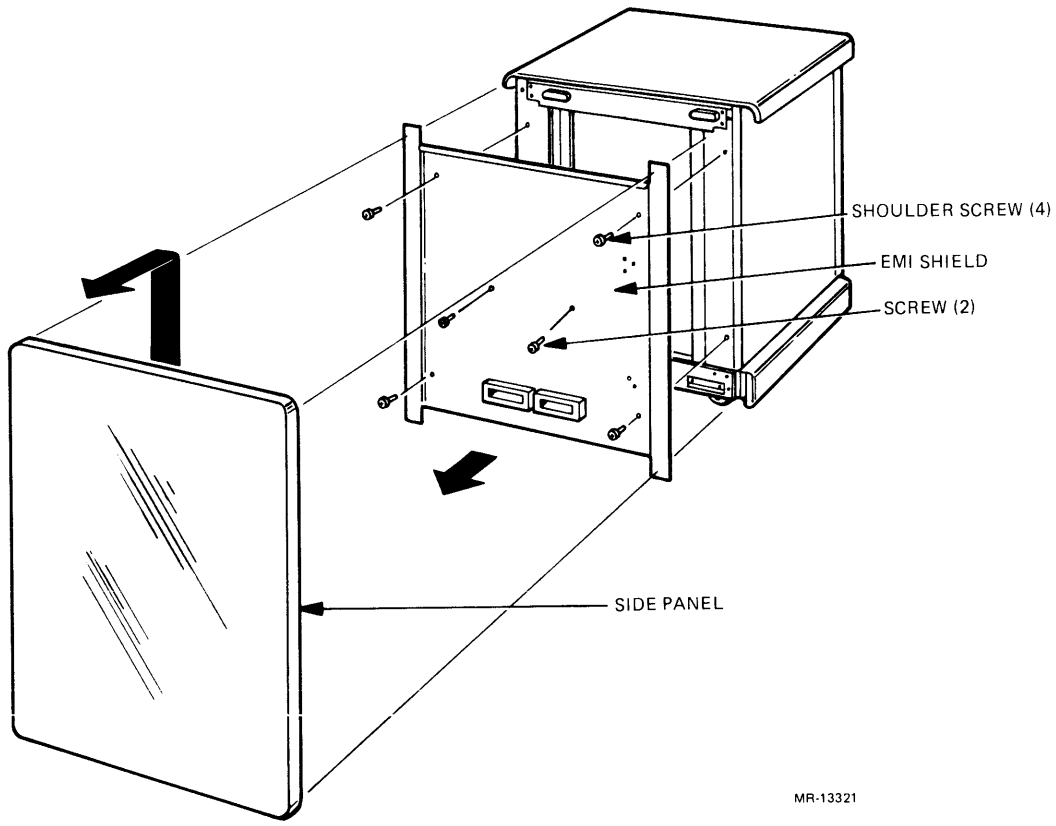

Figure 5-11 Side Panel Removal

10. Remove the two Phillips-head and four shoulder screws securing the EMI panel to the cabinet frame.
11. Carefully lift and line up the BBU enclosure with the four screws protruding from the cabinet frame (Figure 5-12).

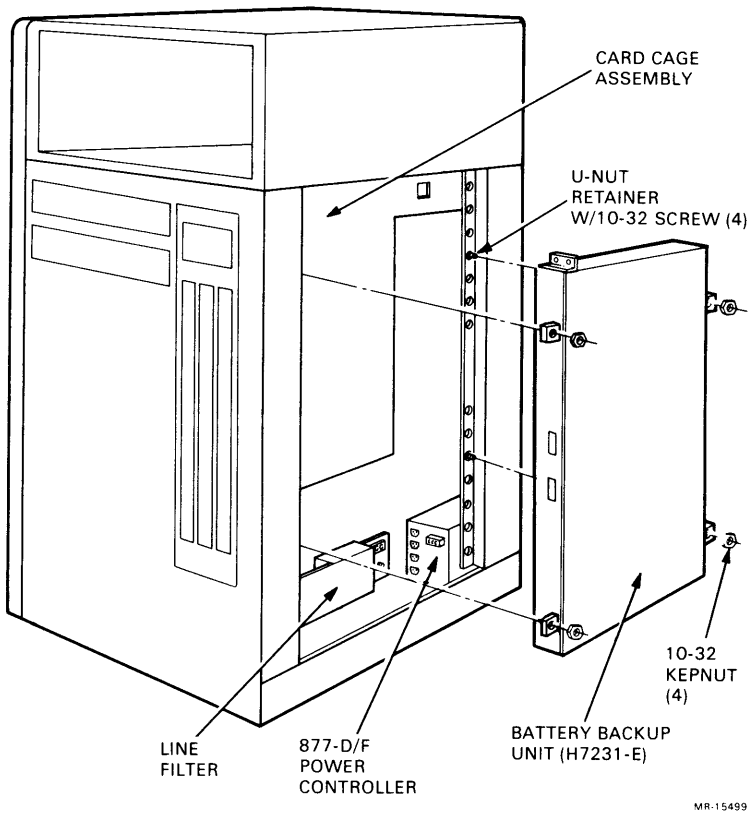

Figure 5-12 Mounting the BBU

12. Position the BBU on the four mounting screws and slide it against the cabinet frame.

13. Install and tighten four 10-32 hex nuts (from the installation kit) on the mounting screws, securing the BBU to the frame.

14. Remove all cables from the installation kit.

15. Install the two-position keyed jumper into mating connector (J20) on the BBU rear panel.

16. Plug one end of the keyed cable (7020396), with ground wire, into the BBU mating connector (J9).

17. Remove the hex nut on the BBU ground stud. Place the ground wire from the cable on the stud. Replace and tighten the hex nut.

18. Plug the other end of the keyed cable, with ground wire, into the line filter bracket connector marked BB-J1. Place the cable ground wire on the stud.

19. Install a 10-32 hex nut (from the installation kit) on the stud. Tighten the nut to secure the ground wire.

20. Plug one end of the other keyed cable (7008288) into the mating BBU power controller bus connector (J19). Plug the other end of the cable into the 877-D/F power controller connector marked either J8 or J9.

21. Plug the ten-position connector of the signal cable (1700730) into the mating polarized connector located at the top right of the card cage assembly.

22. Attach the cable ground wire to the stud with the 10-32 hex nut provided. Secure the wire by tightening the nut.

23. Plug the other end (D-sub) of the cable into the mating connector (J18) on the BBU. Tighten the self-retaining screws on the connector.

24. Plug the appropriate power cord (120 V or 240 V) into the BBU and plug the other end of the cord into the remaining unswitched outlet on the 877-D/F power controller.

25. Check each installed cable to ensure that none were damaged during reinstallation of the EMI shield.

26. Reverse steps 6 through 8 to reinstall the EMI shield and side panel.

This completes the installation procedure.

5.5 BOX BATTERY BACK UP UNIT INSTALLATION

To install the BBU complete the following procedure.

CAUTION
The weight of the BBU is 19 kg (42 lbs); lifting and positioning of the unit requires two people.

1. Unpack the BBU and installation kit.

2. Remove the BBU from the shipping container and place it on a flat surface (Figure 5-13).

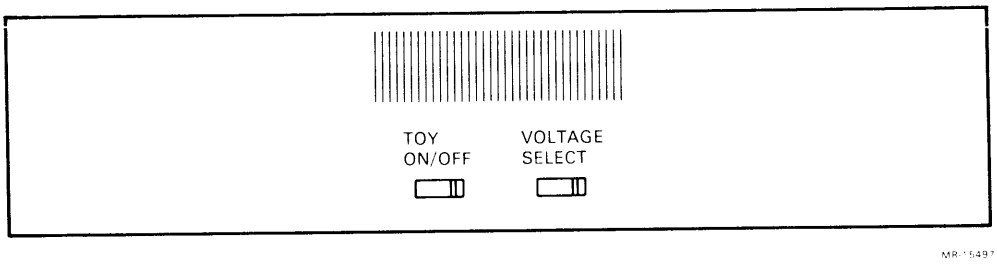

Figure 5-13 BBU Front Panel

3. Set the front panel TOY switch to OFF.

4. Set the VOLTAGE SELECT switch to match the site line voltage.

5. Set the rear BBU AC VOLTAGE SELECT switch to match the front panel VOLTAGE SELECT switch (Figure 5-14).

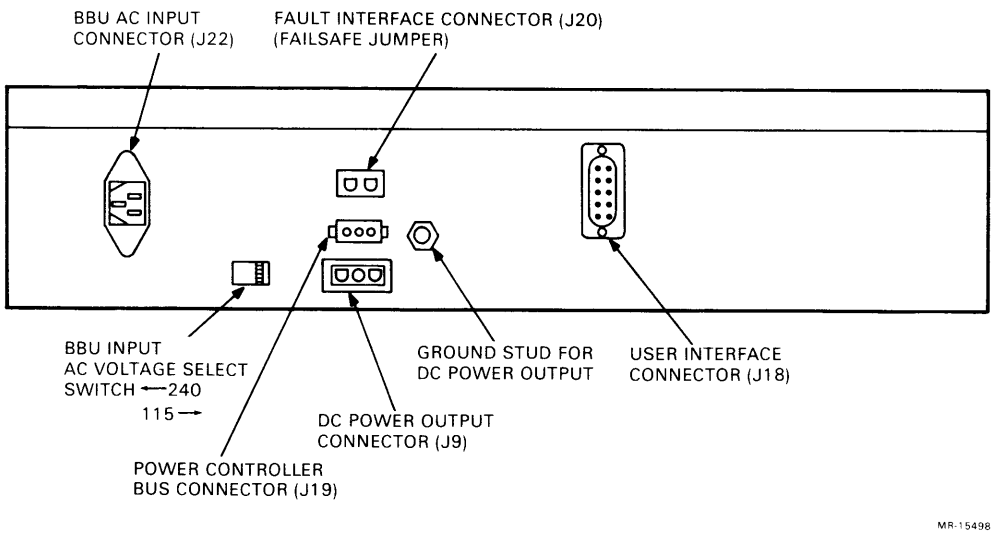

Figure 5-14 BBU Rear Panel

6. Follow the directions supplied with the rack and carefully secure the BBU to the rack.
7. Turn off the box circuit breaker (Figure 5-15).

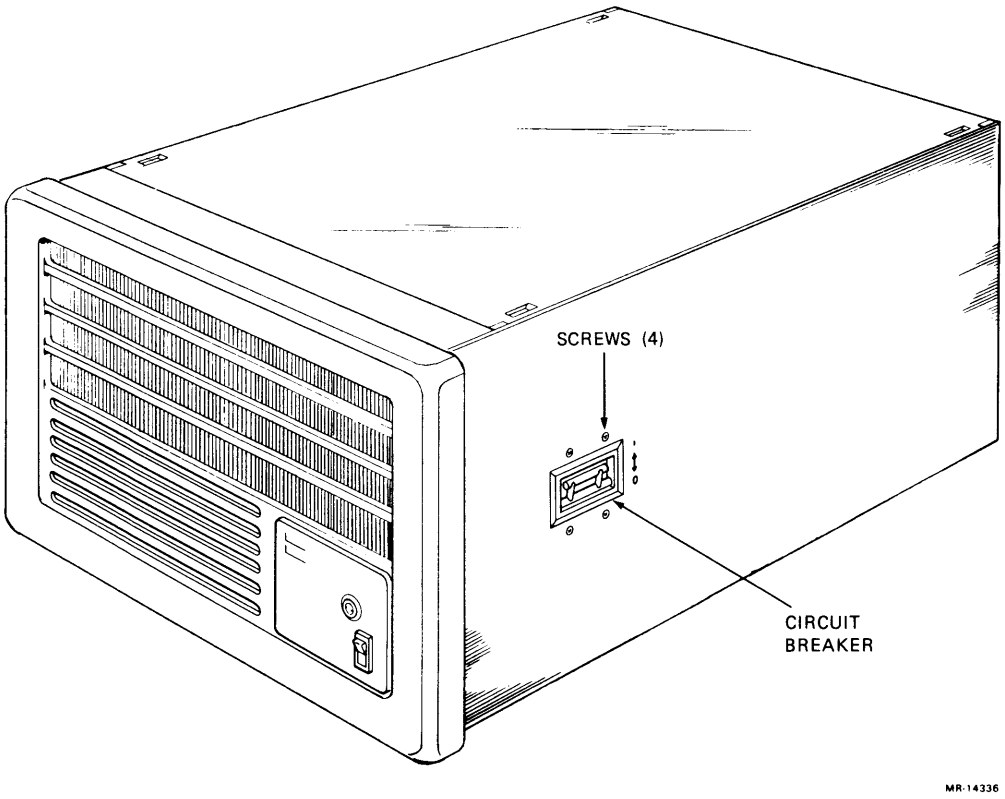

Figure 5-15 Circuit Breaker Location

8. Unplug the ac power cord from the ac outlet.

9. Loosen the four captive screws that secure the box top cover. Remove the cover (Figure 5-16).

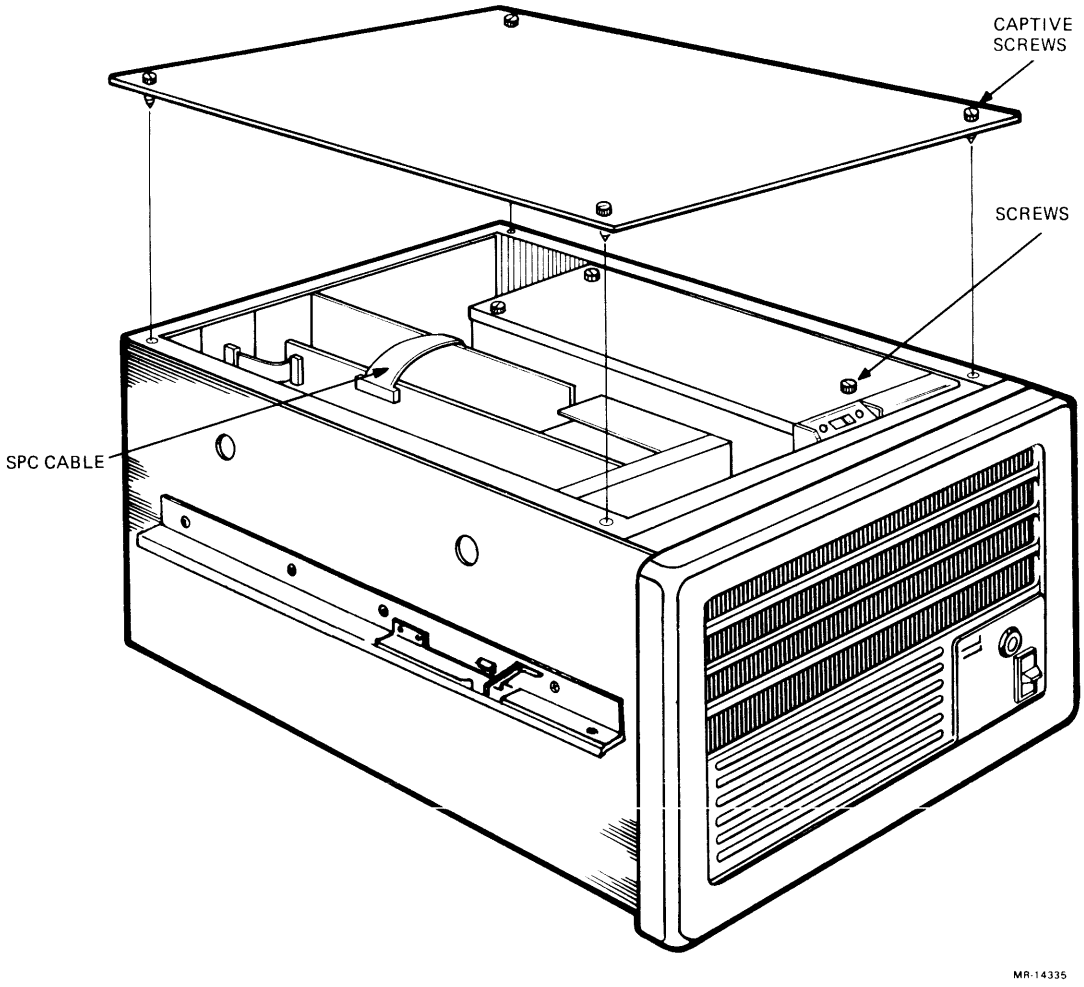

Figure 5-16 Top Cover Removal

10. Remove the blank rear bulkhead panel B1 by loosening the two Phillips-head screws that secure it to the bulkhead (Figure 5-17).

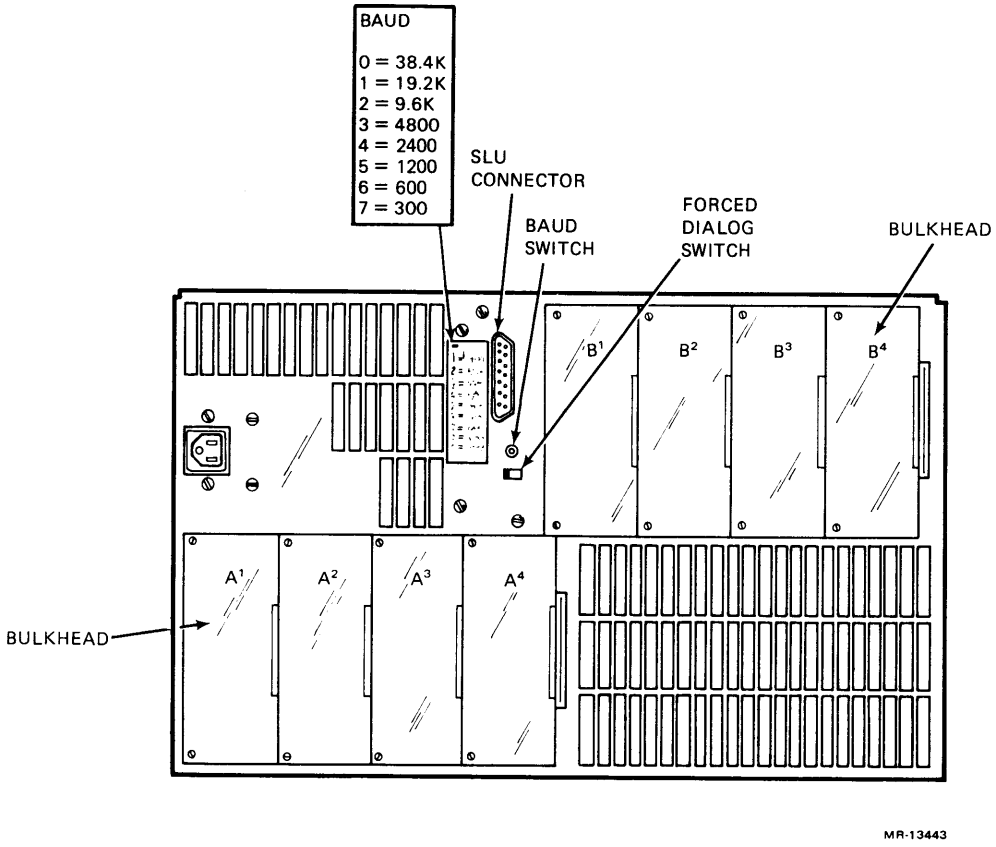

Figure 5-17 Bulkhead Location

11. Remove the BBU panel from the installation kit.

12. Route the two attached cables through the bulkhead opening that was occupied by panel B1.

13. Install the BBU panel (Figure 5-18) in the bulkhead opening and tighten the two flat-head screws into the bulkhead frame.

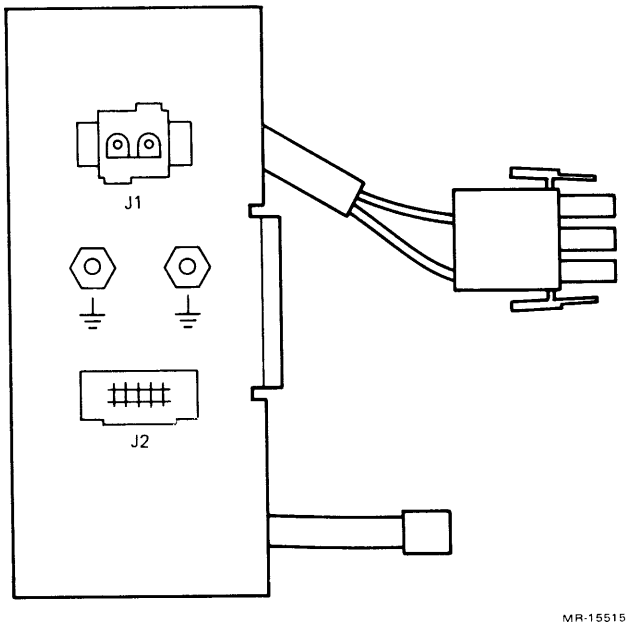

Figure 5-18 BBU Connector Panel

14. Label and remove the cables from the module slot MDM through slot 4.

15. Remove the five modules from the backplane.

16. Plug the signal cable connector (10-position) into the backplane PC board mating connector (J12) (Figure 5-19).

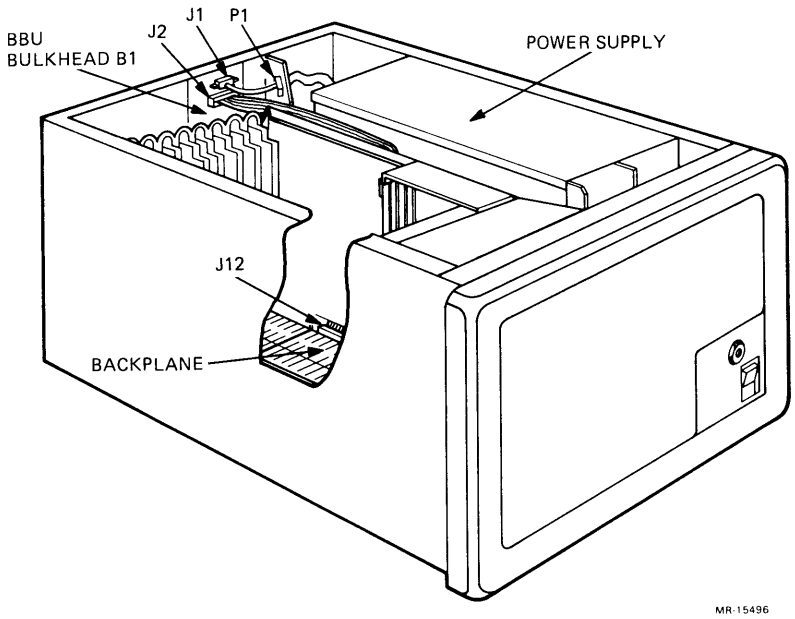

Figure 5-19 BBU Cables and Locations

17. Plug the other BBU cable connector (3 position) into the panel-mounted mating connector located behind the rear of the power supply.

18. Reinstall the five modules. Make certain that they are seated properly in the backplane.

19. Plug the cables into their module connectors.

20. Remove the remaining two cables from the installation kit.

21. Install the two-position keyed jumper into mating connector (J20) on the BBU rear panel (Figure 5-20).

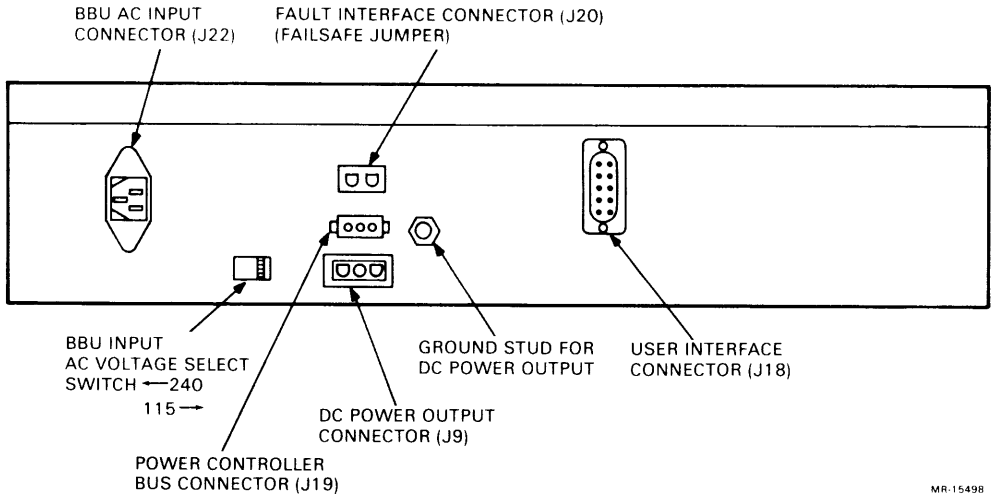

Figure 5-20 BBU Rear Panel

NOTE
BBU connector J19 is not used with this system.

22. Plug one end of the keyed cable (7020396), with ground wire, into the BBU mating connector (J9).

23. Remove the hex nut on the BBU ground stud. Place the ground wire from the cable on the stud. Replace and tighten the hex nut.

24. Plug the other end of the keyed cable, with ground wire, into the BBU bulkhead panel connector (J1). Place the cable ground wire on the stud.

25. Install a 10-32 hex nut (from the installation kit) on the stud. Tighten the nut to secure the ground wire.

26. Plug the signal cable (1700730) into the mating polarized connector located on the BBU bulkhead panel. Attach the cable ground wire to the stud with the 10-32 hex nut provided. Tighten the nut.

27. Plug the other end (D-sub) of the cable into the mating connector on the BBU. Tighten the self-retaining screws on the connector.

28. Replace the top cover of the box and tighten the captive screws.

29. Plug in the appropriate power cord (120 V or 240 V) to the BBU and plug in the other end of the cord to the ac power outlet.

This completes the installation of the BBU.

APPENDIX A
BACKPLANE PIN ASSIGNMENTS

	ROW C		ROW D		ROW E		ROW F	
SIDE / PIN	1	2	1	2	1	2	1	2
A	NPG (IN)	+5V	TP	+5V	GND A	+5V	ABG OUT	+5V
B	NPG (OUT)	15V	TP	15V	ASSYN IN H	15V	ABG IN	15V
C	PA L	GND	A SEL 6	GND	A12 L	GND	SSYN L	GND
D	LTC	D15 L	A OUT LOW	BR7 L	A17 L	A15 L	BBSY L	FO1 N1
E	TP	D14 L	A SEL 4	BR6 L	MSYN L	A16 L	FO1 V2	D02 L
F	TP	D13 L	A SEL 0	BR5 L	A02 L	C1 L	D05 L	D06 L
H	D11 L	D12 L	A IN	BR4 L	A01 L	A00 L	D07 L	A INT ENB B
J	A INT B	D10 L	A SEL 2	A BR OUT	SSYN L	C0 L	NPR L	GND A
K	TP	D09 L	A OUT	BG7 SO	A14 L	A13 L	D08 L	A INT B
L	A INT ENBB	D08 L	INIT L	BG7 OUT	A11 L	TP	D03 L	FO1 L2
M	TP	D07 L	AINT ENBA	BG6 SO	AIN	AOUT HIGH	INTR L	FO1 M2
N	DC LO	D04 L	A INT A	BG6 OUT	A OUT LOW	A08 L	FO1 N1	D04 L
P	HALT REQ	D05 L	TP	BG5 S0	A10 L	A07 L	ABR OUT	FO1 P2
R	HALT GRT	D01 L	TP	BG5 OUT	A09 L	ASEL 4	FO1 L2	FO1 N1
S	PB L	D00 L	TP	BG4 S0	ASEL 6	ASEL 0	FO1 M2	FO1 P2
T	GND	D03 L	GND	BG4 OUT	GND	ASEL 2	GND	SACK L
U	+15	D02 L	TP	ABG IN	A06 L	A04 L	A INT A	ABR OUT
V	AC LO	D06 L	ASSYN IN H	ABG OUT	A05 L	A03 L	A INT ENB A	FO1 FO1

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Figure A-1 SPC Backplane Pin Assignments

STANDARD UNIBUS
PIN DESIGNATIONS

Side / Pin	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	BG6 H	+5V
B	INTR L	GND	BG5 H	GND
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	GND	BR4 L
E	D04 L	D03 L	GND	BG4 H
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	GND	PB L	A11 L	A10 L
P	GND	BBSY L	A13 L	A12 L
R	GND	SACK L	A15 L	A14 L
S	GND	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	NPG H	BR6 L	SSYN L	C0 L
V	BG7 SO	GND	MSYN L	GND

MODIFIED UNIBUS
PIN DESIGNATIONS

SIDE / PIN	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	RESV PIN	+5V
B	INTR L	TP	RESV PIN	TP
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	+5 BAT	BR4 L
E	D04 L	D03 L	INT SSYN	PAR DET
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	PAR P1	PB L	A11 L	A10 L
P	PAR P0	BBSY L	A13 L	A12 L
R	+15 BAT	SACK L	A15 L	A14 L
S	+15 BAT	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	+20 (CORE)	BR6 L	SSYN L	C0 L
V	+20 (CORE)	+20 (CORE)	MSYN L	+5 (CORE)

NOTE: ◪ INDICATES A REDESIGNATED PIN

MR 16204

Figure A-2 Standard and Modified Backplane Pin Assignments

APPENDIX B
WORKSHEET

The purpose of this worksheet is to report and confirm the setup parameters to be contained in the setup EEPROM on the KDJ11-BF CPU module.

Fill out this worksheet when you install a KDJ11-BF CPU module. It will contain all pertinent information for changes made to the setup parameters and programming any future replacement KDJ11-BF CPU modules.

Once filled out, leave it with the system for future use.

Use a pen to fill out the current blocks and pencil for the new blocks.

NOTE

Use SETUP command 1 to exit and SETUP command 7 to list current values (at time of change) and to ensure that the changes you made have been programmed correctly.

Table B-1 SETUP Command 2

		Settings	
Parameters	**Designation**	**Current**	**New**
A - Enable halt on break		=	
B - Disable user friendly format		=	
C - ANSI video terminal		=	
D - Power-up	*	=	
E - Restart	*	=	
F - Ignore battery		=	
G - PMG count	(0-7)	=	
H - Disable clock CSR		=	
I - Force clock interrupts		=	
J - Clock	**	=	
K - Enable ECC test		=	
L - Disable long memory test		=	
M - Disable ROM	***	=	
N - Enable trap on halt		=	
O - Allow alternate boot block		=	
P - Enable UNIBUS memory test		=	
Q - Disable UBA ROM		=	
R - Enable UBA cache (1)		=	
S - Enable 18-bit mode		=	

Designation				
*	0 = Dialog	1 = Automatic	2 = ODT	3 = 24
**	0 = Power supply	1 = 50 Hz	2 = 60 Hz	3 = 800 Hz
***	0 = No	1 = Dis 165	2 = Dis 173	3 = Both
0-7	0 = 0.4 sec	1 = 0.8 sec	through	7 = 25.6 sec
None	0 = No	1 = Yes		

Table B-2 SETUP Command 3

Translation Tables	Current	New
TT1		
Device name	=	
Unit #	=	
CSR address	=	
TT2		
Device name	=	
Unit #	=	
CSR address	=	
TT3		
Device name	=	
Unit #	=	
CSR address	=	
TT4		
Device name	=	
Unit #	=	
CSR address	=	
TT5		
Device name	=	
Unit #	=	
CSR address	=	
TT6		
Device name	=	
Unit #	=	
CSR address	=	
TT7		
Device name	=	
Unit #	=	
CSR address	=	
TT8		
Device name	=	
Unit #	=	
CSR address	=	
TT9		
Device name	=	
Unit #	=	
CSR address	=	

Table B-3 SETUP Command 4

Automatic Boot Device	Current	New
Boot 1	=	
Device name	=	
Boot 2	=	
Device name	=	
Boot 31	=	
Device name	=	
Boot 4	=	
Device name	=	
Boot 5	=	
Device name	=	
Boot 6	=	
Device name	=	

Table B-4 SETUP Command 5
(At the present time, this set-up command is not used.)

	Current	New
Non-English		
0	=	
1	=	
2	=	
3	=	
4	=	
5	=	
6	=	
7	=	
8	=	
9	=	
English		
0	=	
1	=	
2	=	
3	=	
4	=	
5	=	
6	=	
7	=	
8	=	
9	=	

Table B-5 SETUP Command 6
Switches 2, 3, 4

2	3	4	Current	New
ON	ON	ON (Special)	=	
ON	ON	OFF (SB 1)	=	
ON	OFF	ON (SB 2)	=	
ON	OFF	OFF (SB 3)	=	
OFF	ON	ON (SB 4)	=	
OFF	ON	OFF (SB 5)	=	
OFF	OFF	ON (SB 6)	=	
OFF	OFF	OFF (Normal)	=	

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